TENTATIVE TOSHIBA SMALL FORM FACTOR CARD

CompactFlash™ Card

Lead-Free

DESCRIPTION

The THNCFxxxxDGI series CompactFlash™ card is a flash technology based on ATA interface flash memory card. It is constructed with flash disk controller chip and NAND-type flash memory device. The CompactFlash™ card operates in both 5-Volt and 3.3-Volt power supplies. It comes in capacity of 128, 256, 512MB and 1.02GB unformatted for type-I card. Emulating IDE hard disk drives and being certified in accordance with the CompactFlash™ Certification Plan it is a perfect choice of solid-state mass-storage cards for battery backup handheld devices such as Digital Camera, Audio Player, PDA, or industrial application, or the applications that require high environment tolerance with high performance sustained write speed.

FEATURES

- CompactFlash™ Compatibility
  - 3.3V or 5.0V single power supply.
  - 50 pin two piece connector with Type-I form factor (3.3mm Thick)
  - Support for CIS implemented with 256 bytes of attribute memory
- Interface modes
  - PC card memory mode
  - PC card I/O mode
  - True IDE mode
- High performance
  - Interface Transfer speed at PIO mode 4 or Multi Word DMA mode 2 cycle timing, 16.6 Mbytes/second theoretically
  - Sustained write : max 6.0 Mbytes/s in ATA PIO mode 4 cycle timing
  - Sustained read : max 6.5 Mbytes/s in ATA PIO mode 4 cycle timing
- W/E Endurance: 100,000cycles *1 / 300,000cycles *2

  Notes: 1 Ta=-40 to 85°C
  2 Ta= 0 to 70°C

Notes: CompactFlash™ is a trademark of SanDisk Corporation and is licensed royalty-free to the CFA, which in turn will license it royal-free to CFA members.
CFA: CompactFlash™ Association.

Product Specifications

- Line-up:

Card Density	Model No.	Cylinder	Head	Sector	Memory capacity *1
128MB	THNCF128MDGI	978	8	32	128,188,416 Byte
256MB	THNCF256MDGI	978	16	32	256,376,832 Byte
512MB	THNCF512MDGI	993	16	63	512,483,328 Byte
1.02GB	THNCF1G02DGI	1985	16	63	1024,450,560 Byte

*1 : It is the logical address capacity including the area used for File System.

- Dimensions:
  Type I card : 36.4mm(L) x 42.8mm (W) x 3.3mm (H)

- Storage Capacities:
  128MB, 256MB, 512MB and 1.02GB (unformatted)

- Operating Voltage:
  3.3V ± 5%
  5.0V ± 0.5V

- Power consumption:
  - 5V operation
    Active mode:
    Write operation : 28 mA (Typ.)
    Read operation : 23 mA (Typ.)
    Power down mode : 1.2mA (Typ.) 2.0mA (max.)

  - 3.3V operation
    Active mode:
    Write operation : 25 mA (Typ.)
    Read operation : 21 mA (Typ.)
    Power down mode : 1.0mA (Typ.) 1.5mA (max.)

- Environment conditions:
  - Operating temperature: –40°C to 85°C
  - Storage temperature: –45°C to 90°C
  - Storage humidity: 95% (max) (No condensation)

Electrical Interface

- Physical Description:

  The host is connected to the CompactFlash™ Storage Card using a standard 50-pin connector. The connector in the host consists of two rows of 25 male contacts each on 50 mil (1.27 mm) centers.

- Pin Assignments and Pin Type:

  The signal/pin assignments are listed in the section “Pin Assignment and Pin Type”. Low active signals have a “—“ prefix. Pin types are Input, Output or Input/Output. Section “Electrical specification” and “DC characteristics” defines the all input and output type structures.

- Electrical Description:

  The CompactFlash™ Storage Card functions in three basic modes: 1) PC Card ATA using I/O Mode, 2) PC Card ATA using Memory Mode and 3) True IDE Mode, which is compatible with most disk drives. CompactFlash™ Storage Cards are required to support all three modes. The CF Cards normally function in the first and second modes, however they can optionally function in True IDE mode. The configuration of the CompactFlash™ Card will be controlled using the standard PCMCIA configuration registers starting at address 200h in the Attribute Memory space of the storage card. Or for True IDE Mode, pin 9 being grounded. The configuration of the CF Card will be controlled using configuration registers. The configuration registers are starting at the address defined in the Configuration Tuple (CISTPL_CONFIG) in the Attribute Memory space of the CF Card. Signals, whose source is the host, is designated as inputs while signals that the CompactFlash™ Storage Card sources are outputs. The CompactFlash™ Storage Card logic levels conform to those specified in the PC Card Standard Release 8. Each signal has three possible operating modes:

  1) PC Card Memory mode
  2) PC Card I/O mode
  3) True IDE mode

  True IDE mode is required for CompactFlash™ Storage cards. All outputs from the card are totem pole except the data bus signals that are bi-directional tri-state

  As a unique feature, the TOSHIBA CompactFlash™ Storage Card has automatic power down mode. When command process is completed, the card transits to this mode automatically. The card returns to active after receiving next command.

Pin Assignments and Pin Type

PC Card Memory Mode				PC Card I/O Mode				True IDE Mode			
Pin	Signal Name	Pin Type	In, Out Type	Pin	Signal Name	Pin Type	In, Out Type	Pin	Signal Name	Pin Type	In, Out Type
1	GND		Ground	1	GND		Ground	1	GND		Ground
2	D03	I/O	I4Z,OZ1	2	D03	I/O	I4Z,OZ1	2	D03	I/O	I4Z,OZ1
3	D04	I/O	I4Z,OZ1	3	D04	I/O	I4Z,OZ1	3	D04	I/O	I4Z,OZ1
4	D05	I/O	I4Z,OZ1	4	D05	I/O	I4Z,OZ1	4	D05	I/O	I4Z,OZ1
5	D06	I/O	I4Z,OZ1	5	D06	I/O	I4Z,OZ1	5	D06	I/O	I4Z,OZ1
6	D07	I/O	I4Z,OZ1	6	D07	I/O	I4Z,OZ1	6	D07	I/O	I4Z,OZ1
7	–CE1	I	I3U	7	–CE1	I	I3U	7	–CS0	I	I3U
8	A10	I	I3Z	8	A10	I	I3Z	8	A10[2]	I	I3Z
9	–OE	I	I4U	9	–OE	I	I4U	9	–ATA SEL	I	I4U
10	A09	I	I3Z	10	A09	I	I3Z	10	A09[2]	I	I3Z
11	A08	I	I3Z	11	A08	I	I3Z	11	A08[2]	I	I3Z
12	A07	I	I3Z	12	A07	I	I3Z	12	A07[2]	I	I3Z
13	VCC		Power	13	VCC		Power	13	VCC		Power
14	A06	I	I3Z	14	A06	I	I3Z	14	A06[2]	I	I3Z
15	A05	I	I3Z	15	A05	I	I3Z	15	A05[2]	I	I3Z
16	A04	I	I3Z	16	A04	I	I3Z	16	A04[2]	I	I3Z
17	A03	I	I3Z	17	A03	I	I3Z	17	A03[2]	I	I3Z
18	A02	I	I3Z	18	A02	I	I3Z	18	A02	I	I3Z
19	A01	I	I3Z	19	A01	I	I3Z	19	A01	I	I3Z
20	A00	I	I3Z	20	A00	I	I3Z	20	A00	I	I3Z
21	D00	I/O	I4Z,OZ1	21	D00	I/O	I4Z,OZ1	21	D00	I/O	I4Z,OZ1
22	D01	I/O	I4Z,OZ1	22	D01	I/O	I4Z,OZ1	22	D01	I/O	I4Z,OZ1
23	D02	I/O	I4Z,OZ1	23	D02	I/O	I4Z,OZ1	23	D02	I/O	I4Z,OZ1
24	WP	O	OT1	24	–IOIS16	O	OT1	24	–IOIS16	O	ON1
25	–CD2	O	Ground	25	–CD2	O	Ground	25	-CD2	O	Ground
26	–CD1	O	Ground	26	–CD1	O	Ground	26	-CD1	O	Ground
27	D11[1]	I/O	I4Z,OZ1	27	D11[1]	I/O	I4Z,OZ1	27	D11[1]	I/O	I4Z,OZ1
28	D12[1]	I/O	I4Z,OZ1	28	D12[1]	I/O	I4Z,OZ1	28	D12[1]	I/O	I4Z,OZ1
29	D13[1]	I/O	I4Z,OZ1	29	D13[1]	I/O	I4Z,OZ1	29	D13[1]	I/O	I4Z,OZ1
30	D14[1]	I/O	I4Z,OZ1	30	D14[1]	I/O	I4Z,OZ1	30	D14[1]	I/O	I4Z,OZ1
31	D15[1]	I/O	I4Z,OZ1	31	D15[1]	I/O	I4Z,OZ1	31	D15[1]	I/O	I4Z,OZ1
32	–CE2[1]	I	I3U	32	–CE2[1]	I	I3U	32	–CS1[1]	I	I3U
33	–VS1	O	Ground	33	–VS1	O	Ground	33	–VS1	O	Ground
34	–IORD	I	I4U	34	–IORD	I	I4U	34	–DIOR	I	I4U
35	–IOWR	I	I4U	35	–IOWR	I	I4U	35	–DIOW	I	I4U
36	–WE	I	I4U	36	–WE	I	I4U	36	–WE[3]	I	I4U
37	READY	O	OT1	37	–IREQ	O	OT1	37	INTRQ	O	OZ1
38	VCC		Power	38	VCC		Power	38	VCC		Power
39	–CSEL	I	I1U	39	–CSEL	I	I1U	39	–CSEL	I	I1U
40	–VS2	O	OPEN	40	–VS2	O	OPEN	40	–VS2	O	OPEN
41	RESET	I	I3U	41	RESET	I	I3U	41	–RESET	I	I3U

PC Card Memory Mode				PC Card I/O Mode				True IDE Mode			
Pin	Signal Name	Pin Type	In, Out Type	Pin	Signal Name	Pin Type	In, Out Type	Pin	Signal Name	Pin Type	In, Out Type
42	–WAIT	O	OT1	42	–WAIT	O	OT1	42	IORDY	O	ON1
43	–INPACK	O	OT1	43	–INPACK	O	OT1	43	DMARQ	O	OZ1
44	–REG	I	I3U	44	–REG	I	I3U	44	–DMACK	I	I3U
45	BVD2	I/O	I4U,OT1	45	–SPKR	I/O	I4U,OT1	45	–DASP	I/O	I4U,ON1
46	BVD1	I/O	I4U,OT1	46	–STSCHG	I/O	I4U,OT1	46	–PDIAG	I/O	I4U,ON1
47	D08[1]	I/O	I4Z,OZ1	47	D08[1]	I/O	I4Z,OZ1	47	D08[1]	I/O	I4Z,OZ1
48	D09[1]	I/O	I4Z,OZ1	48	D09[1]	I/O	I4Z,OZ1	48	D09[1]	I/O	I4Z,OZ1
49	D10[1]	I/O	I4Z,OZ1	49	D10[1]	I/O	I4Z,OZ1	49	D10[1]	I/O	I4Z,OZ1
50	GND		Ground	50	GND		Ground	50	GND		Ground

Notes: 1. These signals are required only for 16 bit access and not required when installed in 8 bit systems. Devices should allow for 3-state signals not to consume current.
2. Should be grounded by the host.
3. Should be tied to VCC by the host.

Signal Description

Signal Name	Dir	Pin No.	Description
A10 to A0 (PC Card Memory Mode)	I	8,10,11,12,14,15,16,17,18,19,20	Address signals. A10 is the most significant bit, A0 is the least significant bit.
A10 to A0 (PC Card I/O Mode)			
A2 to A0 (True IDE Mode)		18,19,20	In True IDE Mode only A2~0 are available, the remaining address lines should be grounded by the host.
BVD1 (PC Card Memory Mode)	I/O	46	This signal always outputs high, since battery voltage detection is not supported.
−STSCHG (PC Card I/O Mode)			This signal is asserted low to alert the host to changes in the READY and Write Protect states; while the I/O interface is configured. Its use is controlled by the Card Configuration and Status Register.
−PDIAG (True IDE Mode)			In the True IDE Mode, this signal is bi-directional and used to show diagnostic result in the Master/Slave handshake protocol.
BVD2 (PC Card Memory Mode)	I/O	45	This signal always outputs high, since battery voltage detection is not supported.
−SPKR (PC Card I/O Mode)			This is the Binary Audio output signal. Since this card does not support the Binary Audio function, this signal always outputs high.
−DASP (True IDE Mode)			This bi-directional signal is the Disk Active / Slave Present signal.
−CD1, −CD2 (PC Card Memory Mode)	O	26,25	These Card Detect pins are connected to ground on the CompactFlash Storage Card. They are used by the host to determine that the CompactFlash Storage Card is fully inserted into its socket.
−CD1, −CD2 (PC Card I/O Mode)			
−CD1, −CD2 (True IDE Mode)			
−CE1, −CE2 (PC Card Memory Mode)	I	7,32	These input signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed. Please refer to Access specifications.
−CE1, −CE2 (PC Card I/O Mode)			
−CS0, −CS1 (True IDE Mode)			In the True IDE Mode CS0 is the chip select for the task file registers while CS1 is used to select the Alternate Status Register and the Device Control Register.
−CSEL (PC Card Memory Mode)	I	39	This signal is not used for this mode.
−CSEL (PC Card I/O Mode)			
−CSEL (True IDE Mode)			This internally pulled up signal is used to configure this device as a Master or a Slave when configured in the True IDE Mode. When this pin is grounded, this device is configured as a Master. When the pin is open, this device is configured as a Slave.
D15 to D00 (PC Card Memory Mode)	I/O	31,30,29,28,27,49,48,47,6,5,4,3,2,23,22,21	These lines carry the Data, Commands and Status information between the host and the card. D00 is the LSB of the Even Byte of the Word.D08 is the LSB of the Odd Byte of the Word.
D15 to D00 (PC Card I/O Mode)			
D15 to D00 (True IDE Mode)			True IDE Mode, all Task File operations occur in byte mode on the low order bus D00 to D07 while all data transfers are 16 bit using D00 to D15.

Signal Name	Dir	Pin No.	Description
–INPACK (PC Card Memory Mode)	O	43	This signal is not used in this mode. Should not be connected at the host.
–INPACK (PC Card I/O Mode)			The Input Acknowledge signal is asserted by the CompactFlash Storage Card when the card is selected and responding to an I/O read cycle at the address that is on the address bus. This signal is used by the host to control the enable of any input data buffers between the CompactFlash Storage Card and the CPU.
DMARQ (True IDE Mode)			This signal is asserted high when the card is ready to DMA data transfer.
–IORD (PC Card Memory Mode)	I	34	This signal is not used in this mode.
–IORD (PC Card I/O Mode)			This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the CompcatFlash Storage Card when the card is configured to use the I/O interface.
–DIOR (True IDE Mode)			In True IDE Mode, this signal has same function as in PC Card I/O Mode.
–IOWR (PC Card Memory Mode)	I	35	This signal is not used in this mode.
–IOWR (PC Card I/O Mode)			The I/O Write strobe pulse is used to clock I/O data on the Card Data bus into the CompactFlash Storage Card controller registers when the CompactFlash Storage Card is configured to use the I/O interface. The clocking will occur on the negative to positive edge of the signal (trailing edge)
–DIOW (True IDE Mode)			In True IDE Mode, this signal has the same function as in PC Card I/O Mode.
–OE (PC Card Memory Mode)	I	9	This is an Output Enable strobe generated by the host interface .It is used to read data from the CompactFlash Storage Card in Memory Mode and to read the CIS and configuration registers.
–OE (PC Card I/O Mode)			In PC Card I/O Mode, this signal is used to read the CIS and configuration registers.
–ATA SEL (True IDE Mode)			To enable True IDE Mode this input should be grounded by the host .
–REG (PC Card Memory Mode)	I	44	This signal is used during Memory Cycles to distinguish between Common Memory and Attribute Memory accesses. High for Common Memory, Low for Attribute Memory.
–REG (PC Card I/O Mode)			The signal must also be active (low) during I/O Cycles when the I/O address is on the Bus.
–DMACK (True IDE Mode)			This signal is used to indicate DMA transfer request is acknowledged by the host.
READY (PC Card Memory Mode)	O	37	In Memory Mode, this signal is held high when the CompactFlash Storage Card is ready to accept a operation. When the card is busy, this signal is held low. The Host memory card socket must provide a pull-up resistor. At power up or at Reset, the READY signal is held low until the CompactFlash Storage Card has completed its power up or reset function. No access of any type should be made to the CompactFlash Storage Card during this time.
–IREQ (PC Card I/O Mode)			This signal is used as interrupt Request. This line is assert low to indicate a interrupt request is issued.
INTRQ (True IDE Mode)			In True IDE Mode signal is the active high interrupt Request to the host.

Signal Name	Dir	Pin No.	Description
RESET (PC Card Memory Mode)	I	41	When the pin is high, the CompactFlasgh Storage Card is reset. The CompactFlash Storage Card is reset when this pin is left high or open at power up.
RESET (PC Card I/O Mode)			
–RESET (True IDE Mode)			In the True IDE Mode this input pin is the active low hardware reset signal from the host.
GND (PC Card Memory Mode) (PC Card I/O Mode) (True IDE Mode)	—	1,50	Ground
VCC (PC Card Memory Mode) (PC Card I/O Mode) (True IDE Mode)	—	13,38	+5V +3.3V power
–VS1 / –VS2 (PC Card Memory Mode) (PC Card I/O Mode) (True IDE Mode)	O	33,40	Voltage Sense Signals. -VS1 is grounded so that the CompactFlash Storage Card CIS can be read at 3.3 volts and –VS2 is reserved by PCMCIA for a secondary voltage.
–WAIT (PC Card Memory Mode)	O	42	The –WAIT signal is driven low by the CompactFlash Storage Card to indicate the host to delay completion of a memory or I/O cycle that is in progress. This CompactFlash Storage Card outputs always high.
–WAIT (PC Card I/O Mode)			
IORDY (True IDE Mode)			This CompactFlash Storage Card outputs always high.
–WE (PC Card Memory Mode)	I	36	This is a signal driven by the host and used for strobing memory write data to the registers of the CompactFlash Storage Card when the card is configured I the memory interface mode. It is also used for writing the configuration registers.
–WE (PC Card I/O Mode)			In PC Card I/O Mode, this signal is used only for writing the Attribute memory.
–WE (True IDE Mode)			In True IDE Mode this input signal is not used and should be connected to VCC by the host.
WP (PC Card Memory Mode)	O	24	The CompactFlash Storage Card does not have a write protect switch. This signal is held low after the completion of the reset initialization sequence.
–IOIS16 (PC Card I/O Mode)			This signal is asserted when 16 bit or odd byte access to task file registers is accepted.
–IOIS16 (True IDE Mode)			In True IDE Mode this output signal is asserted low when this device is expecting a word data transfer cycle.

Access Specifications

1. Attribute access specifications

When CIS-ROM region or Configuration register region is accessed, read and write operations are executed under the condition of –REG="L" as follows. That region can be accessed by Byte/World/Old-byte modes, which are defined by PC card standard specifications.

- Attribute Read Access Mode

Mode	–REG	–CE2	–CE1	A0	–OE	–WE	D8 to D15	D0 to D7
Standby mode	X	H	H	X	X	X	High-Z	High-Z
Byte access (8bit)	L	H	L	L	L	H	High-Z	even byte
	L	H	L	H	L	H	High-Z	Invalid
Word access (16bit)	L	L	L	X	L	H	invalid	even byte
Odd byte access (8bit)	L	L	H	X	L	H	invalid	High-Z

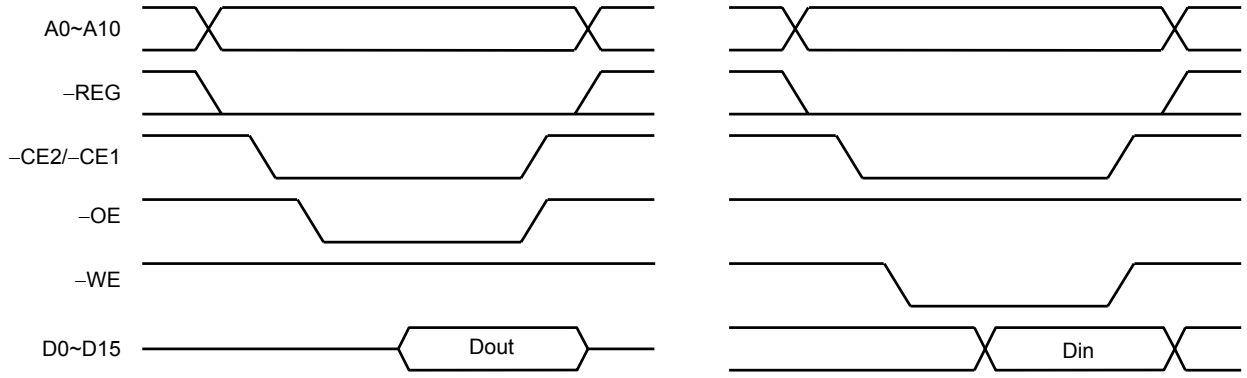
Note: X → L or H

- Attribute Write Access Mode

Mode	–REG	–CE2	–CE1	A0	–OE	–WE	D8 to D15	D0 to D7
Standby mode	X	H	H	X	X	X	Don't care	Don't care
Byte access (8bit)	L	H	L	L	H	L	Don't care	even byte
	L	H	L	H	H	L	Don't care	Don't care
Word access (16bit)	L	L	L	X	H	L	Don't care	even byte
Odd byte access (8bit)	L	L	H	X	H	L	Don't care	Don't care

Note: X → L or H
Write CIS-ROM region is invalid.

- Attribute Access Timing Example



Read cycle Write cycle

2. Task File register access specifications

There are two cases of Task File register mapping, one is mapped I/O address area, the other is mapped Memory address area. Each case of Task File registers read and write operations is executed under the condition as follows. That area can be accessed by Byte/World/Odd Byte modes, which are defined by PC card standard specifications.

- (1) I/O address map

Task File Register Read Access Mode (1)

Mode	–REG	–CE2	–CE1	A0	–IORD	–IOWR	–OE	–WE	D8 to D15	D0 to D7
Standby mode	X	H	H	X	X	X	X	X	High-Z	High-Z
Byte access (8bit)	L	H	L	L	L	H	H	H	High-Z	even byte
	L	H	L	H	L	H	H	H	High-Z	odd byte
Word access (16bit)	L	L	L	X	L	H	H	H	odd byte	even byte
Odd byte access (8bit)	L	L	H	X	L	H	H	H	odd byte	High-Z

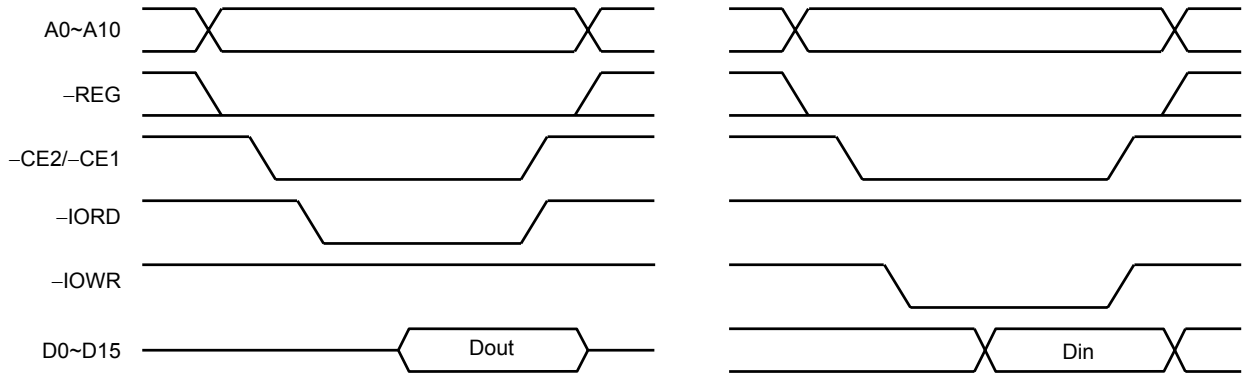
Note: X → L or H

- Task File Register Write Access Mode (1)

Mode	–REG	–CE2	–CE1	A0	–IORD	–IOWR	–OE	–WE	D8 to D15	D0 to D7
Standby mode	X	H	H	X	X	X	X	X	Don't care	Don't care
Byte access (8bit)	L	H	L	L	H	L	H	H	Don't care	even byte
	L	H	L	H	H	L	H	H	Don't care	odd byte
Word access (16bit)	L	L	L	X	H	L	H	H	odd byte	even byte
Odd byte access (8bit)	L	L	H	X	H	L	H	H	odd byte	Don't care

Note: X → L or H

- Task File Register Access Timing Example (1)



Read cycle Write cycle

- (2) Memory address map

Task File Register Read Access Mode (2)

Mode	–REG	–CE2	–CE1	A0	–OE	–WE	–IORD	–IOWR	D8 to D15	D0 to D7
Standby mode	X	H	H	X	X	X	X	X	High-Z	High-Z
Byte access (8bit)	H	H	L	L	L	H	H	H	High-Z	even byte
	H	H	L	H	L	H	H	H	High-Z	odd byte
Word access (16bit)	H	L	L	X	L	H	H	H	odd byte	even byte
Odd byte access (8bit)	H	L	H	X	L	H	H	H	odd byte	High-Z

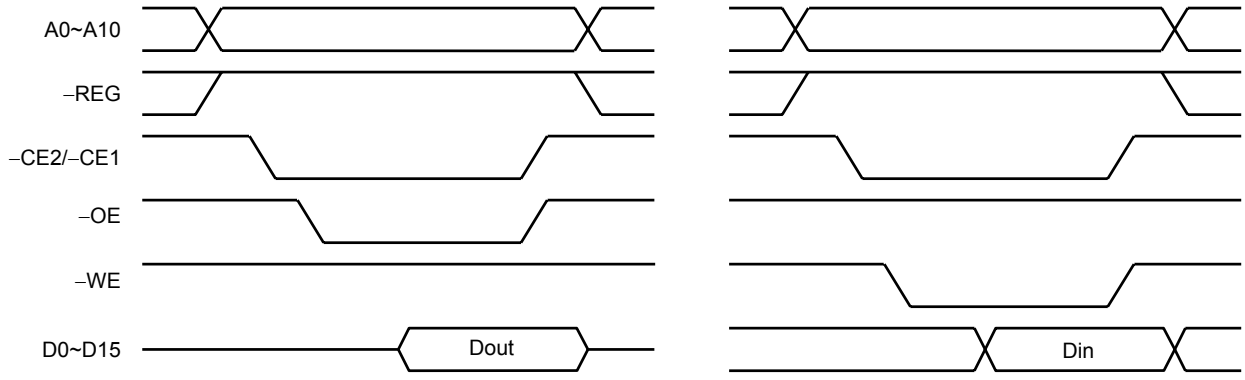
Note: X → L or H

- Task File Register Write Access Mode (2)

Mode	–REG	–CE2	–CE1	A0	–OE	–WE	–IORD	–IOWR	D8 to D15	D0 to D7
Standby mode	X	H	H	X	X	X	X	X	Don't care	Don't care
Byte access (8bit)	H	H	L	L	H	L	H	H	Don't care	even byte
	H	H	L	H	H	L	H	H	Don't care	odd byte
Word access (16bit)	H	L	L	X	H	L	H	H	odd byte	even byte
Odd byte access (8bit)	H	L	H	X	H	L	H	H	odd byte	Don't care

Note: X → L or H

- Task File Register Access Timing Example (2)



Read cycle Write cycle

3. True IDE Mode

The card can be configured in a True IDE This card is configured in this mode only when the-OE input signal is asserted GND by the host while power on. In this True IDE mode Attribute Registers are not accessible from the host. Only I/O operation to the task file and data register is allowed. If this card is configured during power on sequence, data register is accessed in word (16-bit). The card permits 8-bit accessed if the user issues a Set Feature Command to put the device in 8-bit mode.

- True IDE Mode Read I/O Function

Mode	–CE2	–CE1	A0~A2	–DMACK	–DIOR	–DIOW	D8〜D15	D0〜D7
Invalid mode	L	L	X	X	X	X	High-Z	High-Z
Standby mode	H	H	X	H	X	X	High-Z	High-Z
PIO Data register access	H	L	0	H	L	H	Odd byte	even byte
Multiword DMA Data register access	H	H	X	L	L	H	Odd byte	even byte
Alternate status access	L	H	6H	H	L	H	High-Z	Status out
Other task file access	H	L	1~7H	H	L	H	High-Z	Data

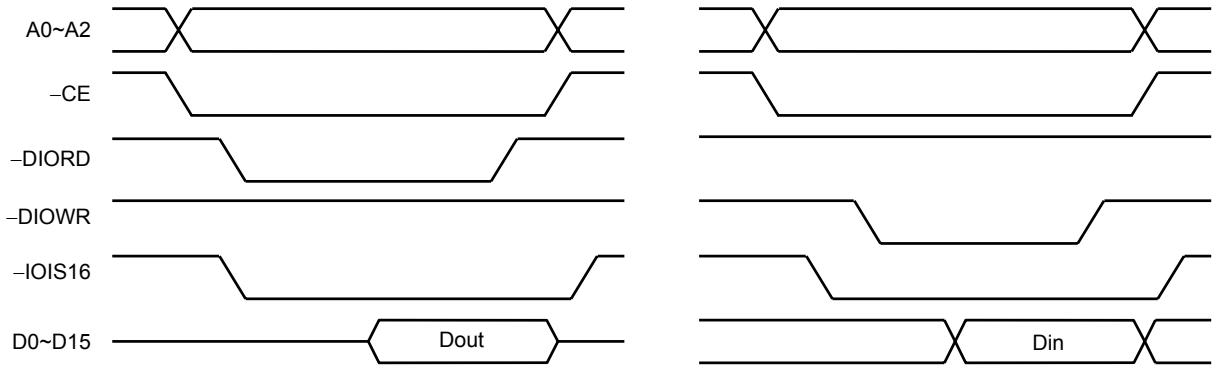
Note: X → L or H

- True IDE Mode Write I/O Function

Mode	–CE2	–CE1	A0~A2	–DMACK	–DIOR	–DIOW	D8〜D15	D0〜D7
Invalid mode	L	L	X	X	X	X	Don't care	Don't care
Standby mode	H	H	X	H	X	X	Don't care	Don't care
PIO Data register access	H	L	0	H	H	L	Odd byte	even byte
Multiword DMA Data register access	H	H	X	L	H	L	Odd byte	even byte
Control register access	L	H	6H	H	H	L	Don't care	Control in
Other task file access	H	L	1~7H	H	H	L	Don't care	Data

Note: X → L or H

- True IDE Mode I/O Access Timing Example



Read cycle Write cycle

Configuration register specifications

This card supports four Configuration registers for the purpose of the configuration and observation of this card. These registers can be used in memory card mode and I/O card mode. In True IDE mode, these registers cannot be used.

1. Configuration Option register (Address 200h)

This register is used for the configuration of the card configuration status and for the issuing soft reset to the card.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
SRESET	LevIREQ	INDEX					

Note: initial value → 00H

Name	R/W	Function
SRESET (HOST->)	R/W	Setting this bit to “1”, places the card in the reset state (Card Hard Reset). This operation is equal to Hard Reset, except this bit is not cleared. Then this bit set to “0”, places the card in the reset state of Hard Reset (This bit is set to “0” by Hard Reset). Card configuration status is reset and the card internal initialized operation starts when Card Hard Reset is executed, so next access to the card should be the same sequence as the power on sequence.
LevIREQ (HOST->)	R/W	This bit sets to “0” when pulse mode interrupt is selected, and “1” when level mode interrupt is selected.
INDEX (HOST->)	R/W	This bits is used for select operation mode of the card as follows. When Power on, Card Hard Reset and Soft Reset, this data is “000000” for the purpose of Memory card interface recognition.

Note: initial value → 00H

- INDEX bit assignment

INDEX bit

5	4	3	2	1	0	Card mode	Task file register address	Mapping mode
0	0	0	0	0	0	Memory card	0H to FH, 400H to 7FFH	Memory mapped
0	0	0	0	0	1	I/O card	xx0H to xxFH	Contiguous I/O mapped
0	0	0	0	1	0	I/O card	1F0H to 1F7H, 3F6H to 3F7H	Primary I/O mapped
0	0	0	0	1	1	I/O card	170H to 177H, 376H to 377H	Secondary I/O mapped

2. Configuration and Status register (Address 202h)

This register is used for observing the state of the card.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
CHGED	SIGCHG	IOIS8	0	0	PWD	INTR	0

Note: initial value → 00H

Name	R/W	Function
CHGED (CARD->)	R	This bit indicates that CREADY bit on Pin Replacement register is set to “1”. When CHGED bit is set to “1”, –STSCHG pin is held “L” at the condition of SIGCHG bit set to “1” and the card configured for the I/O interface.
SIGCHG (HOST->)	R/W	This bit is set or reset by the host for enabling and disabling the status-change signal (–STSCHG pin). When the card is configured I/O card interface and this bit is set “1”, –STSCHG pin is controlled by CHGED bit. If this bit is set to “0”, –STSCHG pin is kept “H”.
IOIS8 (HOST->)	R/W	The host sets this field to “1” when it can provide I/O cycles only with on 8 bit data bus (D7 to D0).
PWD (HOST->)	R/W	When this bit is set to “1”, the card enters sleep state (Power Down mode). When this bit is reset to “0”, the card transfers to idle state (active mode). RREADY bit on Pin Replacement Register becomes BUSY when this bit is changed. RREADY will not become Ready until the power state requested has been entered.
INTR (CARD->)	R	This bit indicates the internal state of the interrupt request. This bit state is available whether I/O card interface has been configured or not. This signal remains true until the condition, which caused the interrupt request, has been serviced. If the –IEN bit in the Device Control Register disables interrupts, this bit is a zero.

3. Pin Replacement register (Address 204H)

This register is used for providing the state of –IREQ signal when the card configured I/O card interface.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	0	CREADY	0	1	1	RREADY	0

Note: initial value → 0CH

Name	R/W	Function
CREADY (HOST->)	R/W	This bit is set to “1” when the RREADY bit changes state. The host may also write this bit.
RREADY (HOST->)	R	When read, this bit indicates +READY pin states. When written, this bit is used for CREADY bit masking.

4. Socket and Copy register (Address 206H)

This register is used for identification of the card from the other cards. Host can read and write this register. Host should set this register before this card's Configuration Option register set.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	0	0	DRV#	0	0	0	0

Note: initial value → 00H

Name	R/W	Function
DRV# (HOST->)	R/W	These fields are used for the configuration of the plural cards. When host configures the plural cards, written the card's copy number in this field. In this way, host can perform the card's master/slave organization.

CIS information

CIS information of Compact Flash card is defined as follows.

Address	Data	Description of contents	CIS function
000H	01H	CISTPL_DEVICE	Tuple code
002H	03H	TPL_LINK	Tuple link
004H	D9H	Device information	Tuple data
006H	01H	Device information	Tuple data
008H	FFH	END MARKER	End of Tuple
00AH	1CH	CISTPL_DEVICE_OC	Tuple code
00CH	04H	TPL_LINK	Tuple link
00EH	03H	Conditions information	Tuple data
010H	D9H	Device information	Tuple data
012H	01H	Device information	Tuple data
014H	FFH	END MARKER	End of Tuple
016H	18H	CISTPL_JEDEC_C	Tuple code
018H	02H	TPL_LINK	Tuple link
01AH	DFH	PCMCIA's manufacturer's JEDEC ID code	Tuple data
01CH	01H	PCMCIA's JEDEC device code	Tuple data
01EH	20H	CISTPL_MANFID	Tuple code
020H	04H	TPL_LINK	Tuple link
022H	98H	Low byte of manufacturer's ID code	Tuple data
024H	00H	High byte of manufacturer's ID code	Tuple data
026H	00H	Low byte of product code	Tuple data
028H	00H	High byte of product code	Tuple data
02AH	15H	CISTPL_VERS_1	Tuple code
02CH	20H	TPL_LINK	Tuple link
02EH	04H	TPLLV1_MAJOR	Tuple data
030H	01H	TPLLV1_MINOR	Tuple data
032H	54H	' T ' (Vender Specific Strings)	Tuple data
034H	4FH	' O ' (Vender Specific Strings)	Tuple data
036H	53H	' S ' (Vender Specific Strings)	Tuple data
038H	48H	' H ' (Vender Specific Strings)	Tuple data
03AH	49H	' I ' (Vender Specific Strings)	Tuple data
03CH	42H	' B ' (Vender Specific Strings)	Tuple data
03EH	41H	' A ' (Vender Specific Strings)	Tuple data
040H	20H	' ' (Vender Specific Strings)	Tuple data
042H	54H	' T ' (Vender Specific Strings)	Tuple data
044H	48H	' H ' (Vender Specific Strings)	Tuple data
046H	4EH	' N ' (Vender Specific Strings)	Tuple data
048H	43H	' C ' (Vender Specific Strings)	Tuple data
04AH	46H	' F ' (Vender Specific Strings)	Tuple data
04CH	X	(Card capacity dependent strings)	Tuple data
04EH	X	(Card capacity dependent strings)	Tuple data
050H	X	(Card capacity dependent strings)	Tuple data
052H	X	(Card capacity dependent strings)	Tuple data
054H	44H	' D ' (Vender Specific Strings)	Tuple data
056H	47H	' G ' (Vender Specific Strings)	Tuple data

Address	Data	Description of contents	CIS function
058H	20H	‘ ’	Tuple data
05AH	00H	Null Terminator	Tuple data
05CH	00H	Reserved (Vender Specific Strings)	Tuple data
05EH	00H	Reserved (Vender Specific Strings)	Tuple data
060H	00H	Reserved (Vender Specific Strings)	Tuple data
062H	00H	Reserved (Vender Specific Strings)	Tuple data
064H	00H	Reserved (Vender Specific Strings)	Tuple data
066H	00H	Reserved (Vender Specific Strings)	Tuple data
068H	00H	Reserved (Vender Specific Strings)	Tuple data
06AH	00H	Reserved (Vender Specific Strings)	Tuple data
06CH	FFH	END MARKER	End of Tuple
06EH	21H	CISTPL_FUNCID	Tuple code
070H	02H	TPL_LINK	Tuple link
072H	04H	IC Card function code	Tuple data
074H	01H	System initialization bit mask	Tuple data
076H	22H	CISTPL_FUNCE	Tuple code
078H	02H	TPL_LINK	Tuple link
07AH	01H	Type of extended data	Tuple data
07CH	01H	Function information	Tuple data
07EH	22H	CISTPL_FUNCE	Tuple code
080H	03H	TPL_LINK	Tuple link
082H	02H	Type of extended data	Tuple data
084H	0CH	Function information	Tuple data
086H	0FH	Function information	Tuple data
088H	1AH	CISTPL_CONFIG	Tuple code
08AH	05H	TPL_LINK	Tuple link
08CH	01H	Size field	Tuple data
08EH	03H	Index number of last entry	Tuple data
090H	00H	Configuration register base address (Low)	Tuple data
092H	02H	Configuration register base address (High)	Tuple data
094H	0FH	Configuration register present mask	Tuple data
096H	1BH	CISTPL_CFTABLE_ENTRY	Tuple code
098H	08H	TPL_LINK	Tuple link
09AH	C0H	Configuration Index Byte	Tuple data
09CH	C0H	Interface Descriptor	Tuple data
09EH	A1H	Feature Select	Tuple data
0A0H	01H	Vcc Selection Byte	Tuple data
0A2H	55H	Nom V Parameter	Tuple data
0A4H	08H	Memory length (256 byte pages)	Tuple data
0A6H	00H	Memory length (256 byte pages)	Tuple data
0A8H	20H	Misc features	Tuple data
0AAH	1BH	CISTPL_CFTABLE_ENTRY	Tuple code
0ACH	06H	TPL_LINK	Tuple link
0AEH	00H	Configuration Index Byte	Tuple data
0B0H	01H	Feature Select	Tuple data
0B2H	21H	Vcc Selection Byte	Tuple data
0B4H	B5H	Nom V Parameter	Tuple data

Address	Data	Description of contents	CIS function
0B6H	1EH	Nom V Parameter	Tuple data
0B8H	4DH	Peak I Parameter	Tuple data
0BAH	1BH	CISTPL_CFTABLE_ENTRY	Tuple code
0BCH	0AH	TPL_LINK	Tuple link
0BEH	C1H	Configuration Index Byte	Tuple data
0C0H	41H	Interface Descriptor	Tuple data
0C2H	99H	Feature Select	Tuple data
0C4H	01H	Vcc Selection Byte	Tuple data
0C6H	55H	Nom V Parameter	Tuple data
0C8H	64H	I/O Parameter	Tuple data
0CAH	F0H	IRQ parameter	Tuple data
0CCH	FFH	IRQ request mask	Tuple data
0CEH	FFH	IRQ request mask	Tuple data
0D0H	20H	Misc features	Tuple data
0D2H	1BH	CISTPL_CFTABLE_ENTRY	Tuple code
0D4H	06H	TPL_LINK	Tuple link
0D6H	01H	Configuration Index Byte	Tuple data
0D8H	01H	Feature Select	Tuple data
0DAH	21H	Vcc Selection Byte	Tuple data
0DCH	B5H	Nom V Parameter	Tuple data
0DEH	1EH	Nom V Parameter	Tuple data
0E0H	4DH	Peak I Parameter	Tuple data
0E2H	1BH	CISTPL_CFTABLE_ENTRY	Tuple code
0E4H	0FH	TPL_LINK	Tuple link
0E6H	C2H	Configuration Index Byte	Tuple data
0E8H	41H	Interface Descriptor	Tuple data
0EAH	99H	Feature Select	Tuple data
0ECH	01H	Vcc Selection Byte	Tuple data
0EEH	55H	Nom V Parameter	Tuple data
0F0H	EAH	I/O parameter	Tuple data
0F2H	61H	I/O range length and size	Tuple data
0F4H	F0H	Base address	Tuple data
0F6H	01H	Base address	Tuple data
0F8H	07H	Address length	Tuple data
0FAH	F6H	Base address	Tuple data
0FCH	03H	Base address	Tuple data
0FEH	01H	Address length	Tuple data
100H	EEH	IRQ parameter	Tuple data
102H	20H	Misc features	Tuple data
104H	1BH	CISTPL_CFTABLE_ENTRY	Tuple code
106H	06H	TPL_LINK	Tuple link
108H	02H	Configuration Index Byte	Tuple data
10AH	01H	Feature Select	Tuple data
10CH	21H	Vcc Selection Byte	Tuple data
10EH	B5H	Nom V Parameter	Tuple data
110H	1EH	Nom V Parameter	Tuple data
112H	4DH	Peak I Parameter	Tuple data

Address	Data	Description of contents	CIS function
114H	1BH	CISTPL_CFTABLE_ENTRY	Tuple code
116H	0FH	TPL_LINK	Tuple link
118H	C3H	Configuration Index Byte	Tuple data
11AH	41H	Interface Descriptor	Tuple data
11CH	99H	Feature Select	Tuple data
11EH	01H	Vcc Selection Byte	Tuple data
120H	55H	Nom V Parameter	Tuple data
122H	EAH	I/O parameter	Tuple data
124H	61H	I/O range length and size	Tuple data
126H	70H	Base address	Tuple data
128H	01H	Base address	Tuple data
12AH	07H	Address length	Tuple data
12CH	76H	Base address	Tuple data
12EH	03H	Base address	Tuple data
130H	01H	Address length	Tuple data
132H	EEH	IRQ parameter	Tuple data
134H	20H	Misc features	Tuple data
136H	1BH	CISTPL_CFTABLE_ENTRY	Tuple code
138H	06H	TPL_LINK	Tuple link
13AH	03H	Configuration Index Byte	Tuple data
13CH	01H	Feature Select	Tuple data
13EH	21H	Vcc Selection Byte	Tuple data
140H	B5H	Nom V Parameter	Tuple data
142H	1EH	Nom V Parameter	Tuple data
144H	4DH	Peak I Parameter	Tuple data
146H	14H	CISTPL_NO_LINK	Tuple code
148H	00H	TPL_LINK	Tuple link
14AH	FFH	CISTPL_END	End of Tuple

Task File Register specification

These registers are used for reading and writing the storage data in this card. These registers are mapped five types by the configuration of INDEX in Configuration Option register. The decoded addresses are shown as follows.

Memory map (INDEX=0)

–REG	A10	A9~A4	A3	A2	A1	A0	Offset	–OE=L	–WE=L
1	0	X	0	0	0	0	0H	Data register	Data register
1	0	X	0	0	0	1	1H	Error register	Feature register
1	0	X	0	0	1	0	2H	Sector count register	Sector count register
1	0	X	0	0	1	1	3H	Sector number register	Sector number register
1	0	X	0	1	0	0	4H	Cylinder low register	Cylinder low register
1	0	X	0	1	0	1	5H	Cylinder high register	Cylinder high register
1	0	X	0	1	1	0	6H	Drive head register	Drive head register
1	0	X	0	1	1	1	7H	Status register	Command register
1	0	X	1	0	0	0	8H	Dup. even data register	Dup. even data register
1	0	X	1	0	0	1	9H	Dup.odd data register	Dup.odd data register
1	0	X	1	1	0	1	DH	Dup.error register	Dup.feature register
1	0	X	1	1	1	0	EH	Alt. status register	Device control register
1	0	X	1	1	1	1	FH	Drive address register	Reserved
1	1	X	X	X	X	0	8H	Even data register	Even data register
1	1	X	X	X	X	1	9H	Odd data register	Odd data register

Contiguous I/O map (INDEX=1)

–REG	A10~A4	A3	A2	A1	A0	Offset	–OE=L	–WE=L
0	X	0	0	0	0	0H	Data register	Data register
0	X	0	0	0	1	1H	Error register	Feature register
0	X	0	0	1	0	2H	Sector count register	Sector count register
0	X	0	0	1	1	3H	Sector number register	Sector number register
0	X	0	1	0	0	4H	Cylinder low register	Cylinder low register
0	X	0	1	0	1	5H	Cylinder high register	Cylinder high register
0	X	0	1	1	0	6H	Drive head register	Drive head register
0	X	0	1	1	1	7H	Status register	Command register
0	X	1	0	0	0	8H	Dup. even data register	Dup. even data register
0	X	1	0	0	1	9H	Dup.odd data register	Dup.odd data register
0	X	1	1	0	1	DH	Dup.error register	Dup.feature register
0	X	1	1	1	0	EH	Alt. status register	Device control register
0	X	1	1	1	1	FH	Drive address register	Reserved

Primary I/O map (INDEX=2)

–REG	A10	A9~A4	A3	A2	A1	A0	–IORD=L	–IOWR=L
0	X	1FH	0	0	0	0	Data register	Data register
0	X	1FH	0	0	0	1	Error register	Feature register
0	X	1FH	0	0	1	0	Sector count register	Sector count register
0	X	1FH	0	0	1	1	Sector number register	Sector number register
0	X	1FH	0	1	0	0	Cylinder low register	Cylinder low register
0	X	1FH	0	1	0	1	Cylinder high register	Cylinder high register
0	X	1FH	0	1	1	0	Drive head register	Drive head register
0	X	1FH	0	1	1	1	Status register	Command register
0	X	3FH	0	1	1	0	Alt. status register	Device control register
0	X	3FH	0	1	1	1	Drive address register	Reserved

Secondary I/O map (INDEX=3)

–REG	A10	A9~A4	A3	A2	A1	A0	–IORD=L	–IOWR=L
0	X	17H	0	0	0	0	Data register	Data register
0	X	17H	0	0	0	1	Error register	Feature register
0	X	17H	0	0	1	0	Sector count register	Sector count register
0	X	17H	0	0	1	1	Sector number register	Sector number register
0	X	17H	0	1	0	0	Cylinder low register	Cylinder low register
0	X	17H	0	1	0	1	Cylinder high register	Cylinder high register
0	X	17H	0	1	1	0	Drive head register	Drive head register
0	X	17H	0	1	1	1	Status register	Command register
0	X	37H	0	1	1	0	Alt. status register	Device control register
0	X	37H	0	1	1	1	Drive address register	Reserved

True IDE Mode I/O map

–CE2	–CE1	A2	A1	A0	-DMACK	–IORD=L	–IOWR=L
1	0	0	0	0	1	PIO Data register	PIO Data register
1	1	X	X	X	0	DMA Data register	DMA Data register
1	0	0	0	1	1	Error register	Feature register
1	0	0	1	0	1	Sector count register	Sector count register
1	0	0	1	1	1	Sector number register	Sector number register
1	0	1	0	0	1	Cylinder low register	Cylinder low register
1	0	1	0	1	1	Cylinder high register	Cylinder high register
1	0	1	1	0	1	Drive head register	Drive head register
1	0	1	1	1	1	Status register	Command register
0	1	1	1	0	1	Alt. status register	Device control register
0	1	1	1	1	1	Drive address register	Reserved

1. Data register

This register is a 16-bit register that has read/write ability, and it is used for transferring 1 sector data between the card and the host. This register can be accessed in word mode and byte mode. This register overlaps the Error or Feature register.

bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
D0 to D15															

2. Error register

This register is a read only register, and it is used for analyzing the error content at the card accessing. This register is valid when the BSY bit in Status register and Alternate Status register are set to "0"(Ready).

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
BBK	UNC	0	IDNF	0	ABRT	0	AMNF

bit	Name	Function
7	BBK(Bad Block detected)	This bit is set when a Bad Block is detected in requester ID field.
6	UNC(Data ECC error)	This bit is set when Uncorrectable error is occurred at reading the card.
4	IDNF(ID Not Found)	The requested sector ID is in error or cannot be found.
2	ABRT(ABoRTed command)	This bit is set if the command has been aborted because of the card status condition.(Not ready, Write fault, Invalid command, etc.)
0	AMNF(Address Mark Not Found)	This bit is set in case of a general error.

3. Feature register

This register is write-only register, and provides information regarding features of the drive that the host wishes to utilize.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Feature byte							

4. Sector count register

This register contains the numbers of sectors of data requested to be transferred on a read or write operation between the host and the card. If the value of this register is zero, a count of 256 sectors is specified. In plural sector transfer, if not successfully completed, the register contains the number of sectors, which need to be transferred in order to complete, the request.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Sector count byte							

5. Sector number register

This register contains the starting sector number, which is started by following sector transfer command.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Sector number byte (CHS mode) / LBA 07 – 00 (LBA mode)							

6. Cylinder low register

This register contains the low 8-bit of the starting cylinder address, which is started by following sector transfer command.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Cylinder low byte (CHS mode) / LBA 15 – 08 (LBA mode)							

7. Cylinder high register

This register contains the high 8-bit of the starting cylinder address, which is started by following sector transfer command.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Cylinder high byte (CHS mode) / LBA 23 – 16 (LBA mode)							

8. Drive head register

This register is used for selecting the Drive number and Head number for the following command.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Obsolete	LBA	Obsolete	DRV	Head number (CHS mode) / LBA 27 ~ 24 (LBA mode)			

bit	Name	Function
7	Obsolete (1)	This bit is normally set to “1”.
6	LBA	LBA is a flag to select either Cylinder/Head/Sector (CHS) or Logical Block Address (LBA) mode. When LBA = 0, CHS mode is selected. When LBA=1, LBA mode is selected
5	Obsolete (1)	This bit is normally set to “1”.
4	DRV (Drive select)	This bit is used for selecting the Master (DRV=0) or Slave (DRV=1) in Master/Slave organization.
3~0	Head number	This bit is used for selecting the Head number in CHS mode or LBA 27~24 in LBA mode for the following command. Bit 3 is MSB.

9. Status register

This register is read only register, and it indicates the card status of command execution. When this register is read in configured I/O card mode (INDEX=1,2,3) and level interrupt mode, –IREQ is negated.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR

bit	Name	Function
7	BSY (BuSY)	This bit is set when the card internal operation is executing. When this bit is set to “1”, other bits in this register are invalid.
6	DRDY (Drive ReaDY)	If this bit and DSC bit are set to “1”, the card is capable of receiving the read or write or seek requests. If this bit is set to “0”, the card prohibits these requests.
5	DWF (Drive Write Fault)	This bit is set if this card indicates the write fault status.
4	DSC (Drive Seek Complete)	This bit is set when the drive seeks complete.
3	DRQ (Data ReQuest)	This bit is set when the information can be transferred between the host and Data register. This bit is cleared when the card receives the other command.
2	CORR (CORRected data)	This bit is set when a correctable data error has been occurred and the data has been corrected.
1	IDX (InDeX)	This bit is always set to “0”.
0	ERR (ERRor)	This bit is set when the previous command has ended in some type of error. The error information is set in the error register. This bit is cleared by the next command.

10. Alternate status register

This register is the same as Status register in physically, so the bit assignment refers to previous item of Status register. But this register is different from Status register that –IREQ is not negated when data read.

11. Command register

This register is write only register, and it is used for writing the command to execute the requested operation. The command code is written in the command register, after the parameter is written in the Task File register when the card is in Ready state.

12. Device control register

This register is write only register, and it is used for controlling the card interrupt request and issuing an ATA soft reset to the card.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
X	X	X	X	1	SRST	nIEN	0

bit	Name	Function
7 to 4	X	Don't care
3	1	This bit is set to "1".
2	SRST(Software ReSeT)	This bit is set to "1" in order to force the card to perform Task File Reset operation. This does not change the Card Configuration registers as a Hardware Reset does. The card remains in Reset until this bit is reset to "0".
1	nIEN(Interrupt Enable)	This bit is used for enabling –IREQ. When this bit is set to "0", –IREQ is enabled. When this bit is set to "1", –IREQ is disabled.
0	0	This bit is set to "0".

13. Drive Address register

This register is read only register, and it is used for confirming the drive status. This register is provides for compatibility with the AT disk drive interface. It is recommended that this register is not mapped into the host's I/O space because of potential conflicts on bit7.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
X	nWTG	nHS3	nHS2	nHS1	nHS0	nDS1	nDS0

bit	Name	Function
7	X	This bit remains tri-state when host read access.
6	nWTG (WriTing Gate)	This bit is set as 0
5 to 2	NHS3 to nHS0 (Head Select3-0)	These bits are the negative value of Head Select bits (bit3 to 0) in Drive/Head register.
1	nDS1 (Idrive Select1)	This bit is 0 when drive 1 is active and selected.
0	nDS0 (Idrive Select0)	This bit is 0 when drive 0 is active and selected.

ATA Command specifications

This table summarizes the ATA command set with the paragraphs. Following shows the supported commands and command codes, which are written in command registers.

ATA Command Set

Command set	Code	FR	SC	SN	CY	DR	HD	LBA
Check power mode	E5h or 98h	—	—	—	—	Y	—	—
Execute drive diagnostic	90H	—	—	—	—	Y	—	—
Erase sector(s)	C0H	—	Y	Y	Y	Y	Y	Y
Format track	50H	—	Y	—	Y	Y	Y	Y
Identify Drive	ECH	—	—	—	—	Y	—	—
Idle	E3h or 97h	—	Y	—	—	Y	—	—
Idle immediate	E1h or 95h	—	—	—	—	Y	—	—
Initialize drive parameters	91H	—	Y	—	—	Y	Y	—
Read buffer	E4H	—	—	—	—	Y	—	—
Read DMA	C8H	—	Y	Y	Y	Y	Y	Y
Read multiple	C4H	—	Y	Y	Y	Y	Y	Y
Read long sector	22H or 23H	—	—	Y	Y	Y	Y	Y
Read sector (s)	20H or 21H	—	Y	Y	Y	Y	Y	Y
Read verify sector (s)	40H or 41H	—	Y	Y	Y	Y	Y	Y
Recalibrate	1XH	—	—	—	—	Y	—	—
Request sense	03H	—	—	—	—	Y	—	—
Seek	7XH	—	—	Y	Y	Y	Y	Y
Set features	EFH	Y	—	—	—	Y	—	—
Set multiple mode	C6H	—	Y	—	—	Y	—	—
Set sleep mode	E6h or 99h	—	—	—	—	Y	—	—
Stand by	E2h or 96h	—	—	—	—	Y	—	—
Stand by immediate	E0h or 94h	—	—	—	—	Y	—	—
Translate sector	87H	—	Y	Y	Y	Y	Y	Y
Wear level	F5H	—	—	—	—	Y	Y	—
Write buffer	E8H	—	—	—	—	Y	—	—
Write DMA	CAH	—	Y	Y	Y	Y	Y	Y
Write long sector	32H or 33H	—	—	Y	Y	Y	Y	Y
Write multiple	C5H	—	Y	Y	Y	Y	Y	Y
Write multiple w/o erase	CDH	—	Y	Y	Y	Y	Y	Y
Write sector	30H or 31H	—	Y	Y	Y	Y	Y	Y
Write sector w/o erase	38H	—	Y	Y	Y	Y	Y	Y
Write verify	3CH	—	Y	Y	Y	Y	Y	Y

Notes: FR: Feature register
SC: Sector Count register (00H~FFH)
SN: Sector Number register (01H~20H)
CY: Cylinder Low / High register
DR: Drive bit of Drive / Head register
HD: Head No.(0~3) of Drive / Head register
LBA: Logical Block Address Mode supported
Y: Set up
—: Not set up

(1) Check Power Mode (code: E5h or 98h):

This command checks the power mode.

(2) Execute Drive Diagnostic (code: 90h):

This command performs the internal diagnostic tests implemented by the Card.

(3) Erase Sector(s)(code: C0h):

This command is used to erase data sectors, but sector data is not erased in this product.

(4) Format Track (code: 50h):

This command writes the desired head and cylinder of the selected drive with a vendor unique data pattern (typically FFh or 00h). To remain host backward compatible, the card expects one sector (512Bytes) of data from the host to follow the command with same protocol as the Write Sector Command.

(5) Identify Drive (code: ECh):

This command enables the host to receive the Identify Drive Information from the card.

Identify Drive Information

Word address	Default value	Total bytes	Data field type information
0	X4XAH	2	General configuration bit-significant information. PC card (memory, I/O) mode : 848Ah, IDE mode: 044Ah.
1	XXXX	2	Default number of cylinders
2	0000H	2	Reserved
3	00XXH	2	Default number of heads
4	XXXX	2	Number of unformatted bytes per track
5	XXXX	2	Number of unformatted bytes per sector
6	XXXX	2	Default number of sectors per track
7～8	XXXX	4	Number of sectors per card(Word7=MSW, Word8=LSW)
9	0000H	2	Reserved
10～19	XXXX	20	Serial number in ASCII
20	0001H	2	Buffer type (single ported)
21	0004H	2	Buffer size in 512 byte increments
22	0004H	2	# of ECC bytes passed on Read/Write Long Commands
23～26	XXXX	8	Firmware revision in ASCII.
27～46	XXXX	40	Model number in ASCII.
47	8001H	2	Maximum of 1 sector on Read/Write Multiple command
48	0000H	2	Double Word not supported
49	0F00H	2	Capabilities: DMA supported(bit 8), LBA supported (bit9)
50	0000H	2	Reserved
51	0200H	2	PIO data transfer cycle timing mode 2
52	0000H	2	DMA data transfer cycle timing mode (Obsolete in ATA3 and later)
53	0003H	2	Field validity (Word54~58 and Word 64~70 are valid)
54	XXXX	2	Current number of cylinders.
55	XXXX	2	Current number of heads
56	XXXX	2	Current sectors per track
57~58	XXXX	4	Current capacity in sectors
59	0101H	2	Multiple sector setting is valid
60 ~ 61	XXXX	4	Total number of sectors addressable in LBA Mode
62	0000H	2	(obsolete)
63	0407H	2	Multiword DMA: mode2~0 supported (bit2~0), mode2 selected (bit10)
64	0003	2	Advanced PIO modes supported. Mode4,3 are supported (bit1,0)
65~68	XXXX	8	multiword DMA and PIO cycle time in nano seconds.
69～255	0000H	374	Reserved

(6) Idle (code: E3h or 97h):

This command causes the Card to set BSY, enter the Idle mode, clear BSY and generate an interrupt. If sector count is non-zero, the automatic power down mode is enabled. If the sector count is zero, the automatic power mode is disabled.

(7) Idle Immediate (code: E1h or 95h):

This command causes the Card to set BSY, enter the Idle(Read) mode, clear BSY and generate an interrupt.

(8) Initialize Drive Parameters (code: 91h):

This command enables the host to set the number of sectors per track and the number of heads per cylinder.

(9) Read Buffer (code: E4h):

This command enables the host to read the current contents of the card's sector buffer.

(10) Read DMA (code: C8h) :

This command reads from 1 to 256 sectors as specified in the Sector Count register using the DMA data transfer protocol. A sector count of zero requests 256 sectors. The transfer beings at the sector specified in the Sector Number register.

(11) Read Multiple (code: C4h):

This command performs similarly to the Read Sectors command. Interrupts are not generated on each sector, but on the transfer of a block, which contains the number of sectors defined by a Set Multiple command.

(12) Read Long Sector (code 22h or 23h):

This command performs similarly to the Read Sector(s) command except that it returns 516 bytes of data instead of 512 bytes.

(13) Read Sector(s) (code 20h or 21h):

This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer beings specified in the Sector Number register.

(14) Read Verify Sector(s) (code: 40h or 41h):

This command is identical to the Read Sectors command, except that DRQ is never set and no data is transferred to the host.

(15) Recalibrate (code: 1Xh):

This command is effectively a NOP command to the Card and is provided for compatibility purposes.

(16) Request Sense (code: 03h):

This command requests an extended error code after command ends with an error.

(17) Seek (code: 7Xh):

This command is effectively a NOP command to the Card although it does perform a range check.

(18) Set Features (code: EFh):

This command is used by the host to establish or select certain features.

Features	Operation
01H	Enable 8-bit data transfers.
03H	Set transfer mode base on value in sector count register
05H	Enable Advanced Power Management
09H	Enable Extended Power operations.
0AH	Enable Level 1 commands
44H	Product specific ECC bytes apply on Read/Write Long commands
55H	Disable Read Look Ahead.
66H	Disable Power on Reset (POR) establishment of defaults at Soft Reset.
69H	NOP – Accepted for backward compatibility
81H	Disable 8-bit data transfers.
85H	Disable Advanced Power Management
89H	Disable Extended Power operations
8AH	Disable Power Level 1 commands
96H	NOP – Accepted for backward compatibility
97H	Accepted for backward compatibility. Use od this Feature is not recommended.
9AH	Set the host current source capability. Allows tradeoff between current drawn and read/write speed
BBH	4 bytes of data apply on Read/Write Long commands.
CCH	Enable Power on Reset (POR) establishment of defaults at Soft Reset.

(19) Set Multiple Mode (code: C6h):

This command enables the Card to perform Read and Write Multiple operations and establishes the block count for these commands.

(20) Set Sleep Mode (code: E6h or 99h):

This command causes the Card to set BSY, enter the Sleep mode, clear BSY and generate an interrupt.

(21) Stand By (code: E2h or 96h):

This command causes the Card to set BSY, enter the Sleep mode (which corresponds to the ATA "Standby" Mode), clear BSY and return the interrupt immediately.

(22) Stand By Immediate (code: E0h or 94h):

This command causes the Card to set BSY, enter the Sleep mode (which corresponds to the ATA "Standby" Mode), clear BSY and return the interrupt immediately.

(23) Translate Sector (code: 87h):

This command effectively a NOP command and only implemented for backward compatibility.

(24) Wear Level (code: F5h):

This command effectively a NOP command and only implemented for backward compatibility. The Sector Count Register will always be returned with a 00h indicating Wear Level is not needed.

(25) Write Buffer (code: E8h):

This command enables the host to overwrite contents of the Card's sector buffer with any data pattern desired.

(26) Write DMA (code: CAh):

This command writes from 1 to 256 sectors as specified in the Sector Count register using the DMA data transfer protocol. A sector count of zero requests 256 sectors. The transfer begins at the sector specified in the Sector Number register

(27) Write Long Sector (code: 32h or 33h):

This command is provided for compatibility purposes and is similar to the Write Sector(s) command except that it writes 516 bytes instead of 512 bytes.

(28) Write Multiple (code: C5h):

This command is similar to the Write Sectors command. Interrupts are not presented on each sector, but on the transfer of a block which contains the number of sectors defined by Set Multiple command.

(29) Write Multiple without Erase (code: CDh):

This command is similar to the Write Multiple command with the exception that an implied erase before write operation is not performed.

(30) Write Sector(s): (code: 30h or 31h):

This command writes from 1 to 256 sectors as specified in the Sector Count register. A sector count of zero requests 256 sectors. The transfer begins at the sector specified in the Sector Number register.

(31) Write Sector(s) without Erase (code: 38h):

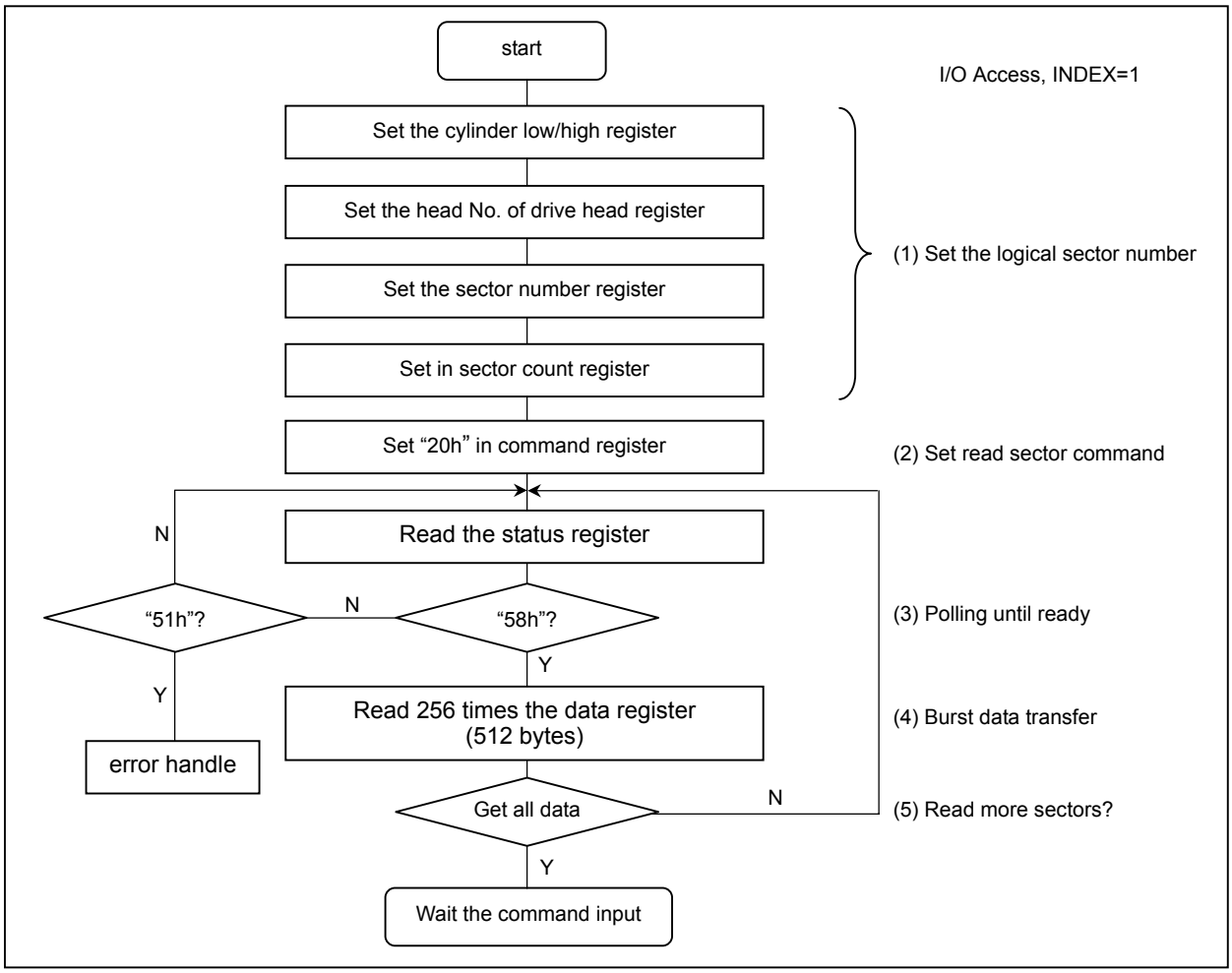
This command is similar to the Write Sector(s) command with the exception that an implied erase before write operation is not performed.

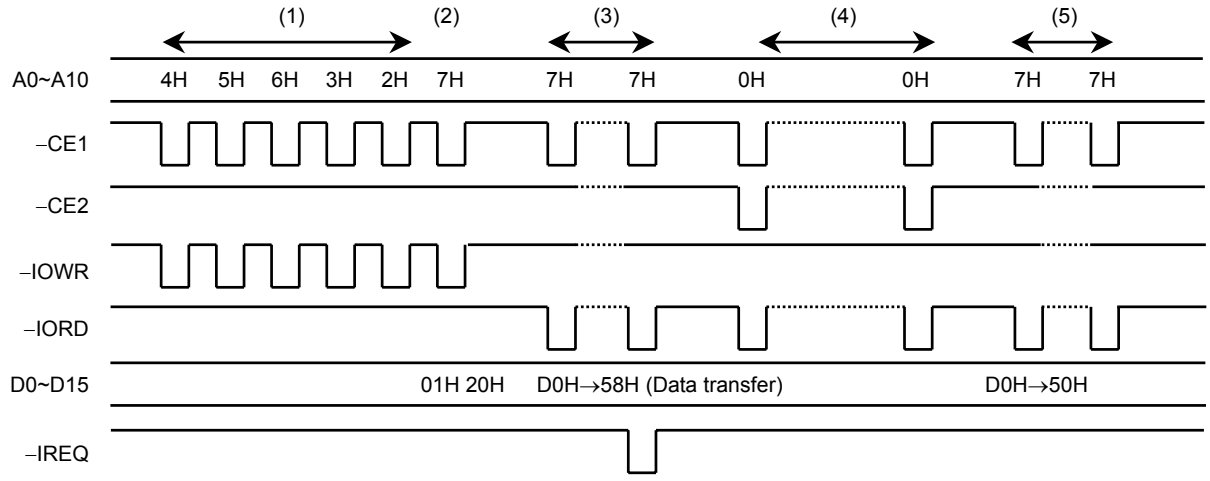
(32) Write Verify (code: 3Ch):

This command is similar to the Write Sector(s) command, except each sector is verified immediately after being written.

Sector Transfer Protocol

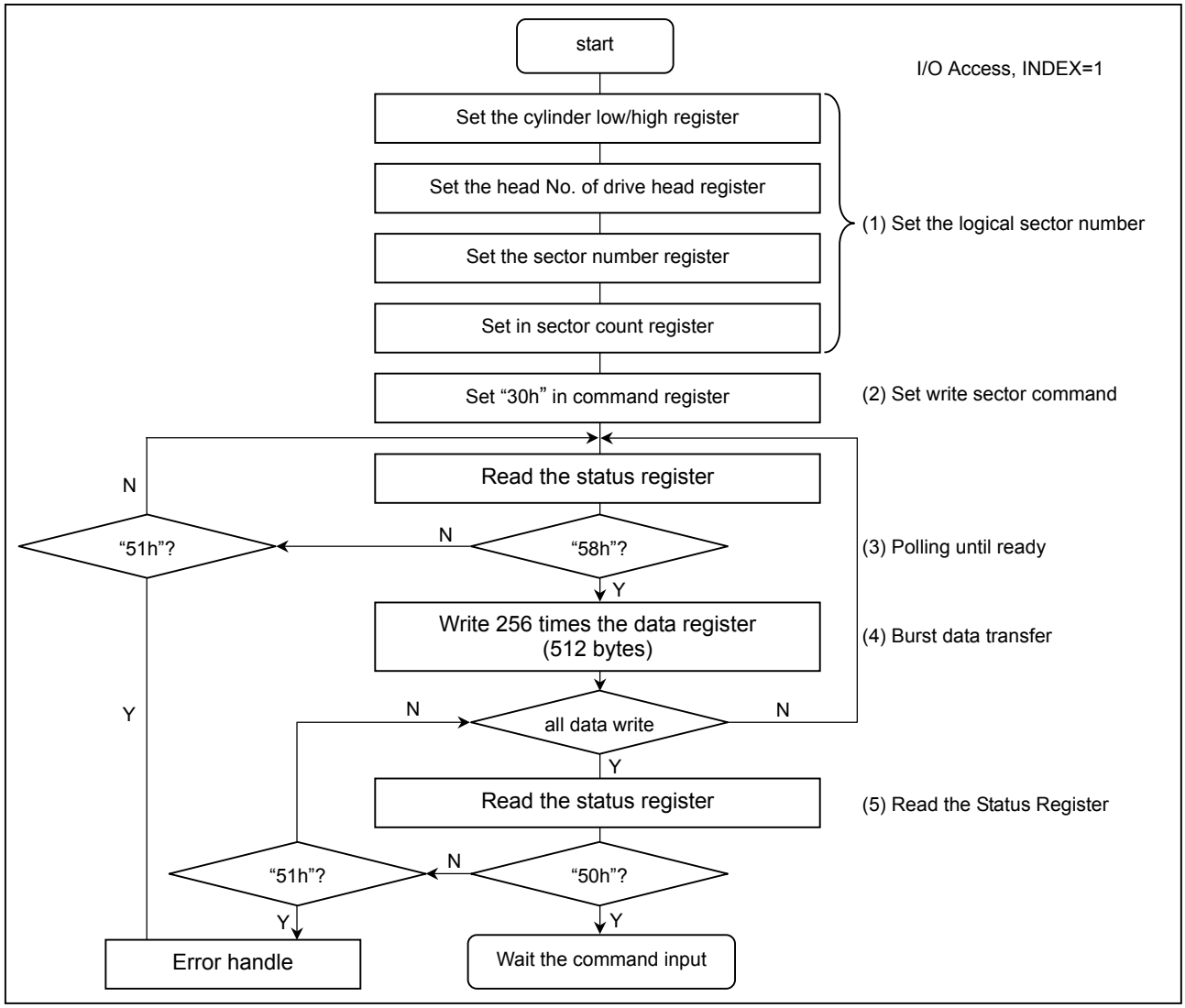
1. Sector read: Sector read procedure after the card configured I/O interface is shown as follows.

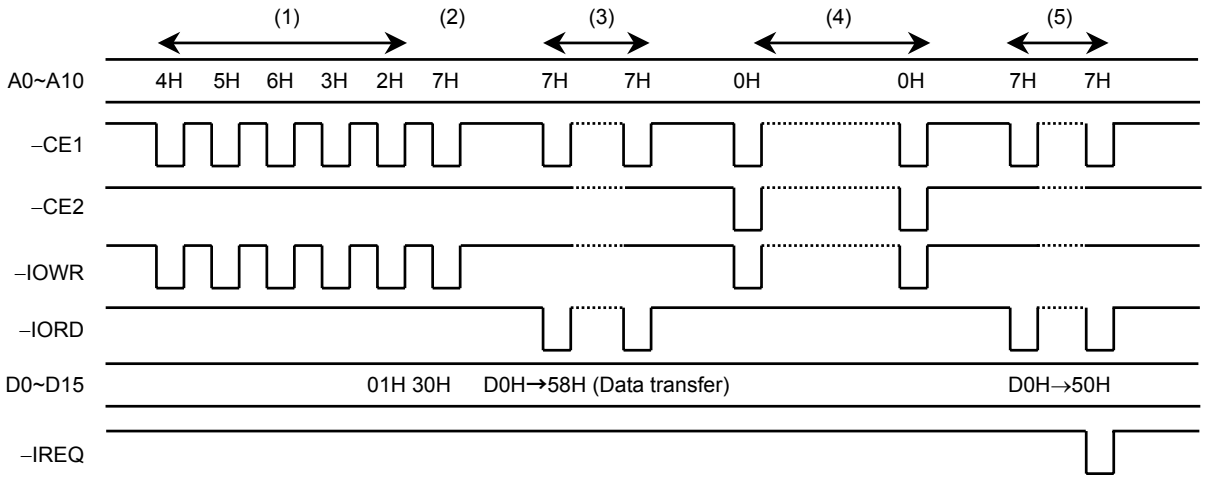




Note: If sector count is not equal to 1, the busy time (status is "DXH") maybe only 1μs, so if host handle step (3) by polling status "DXH" then polling status "58H", it could be generated "time out error" because it can not get status "DXH".

2. Sector write: write sector procedure after the card configured I/O interface is shown as follows.





Note: If sector count is not equal to 1, the busy time (status is "DXH") maybe only 1μs, so if host handle step (3) by polling status "DXH" then polling status "58H", it could be generated "time out error" because it can not get status "DXH".

Card System performance

ITEM	Performance
Set up time (Reset to Ready)	250 ms (max.)
Set up time (Power down to Ready)	5.5 ms (max.)
Data transfer rate to / from host	16.6 M byte / s burst (max.), theoretically
Sustained read transfer rate	6.5 M byte / s (max.), actually *1
Sustained write transfer rate	6.0 M byte / s (max.), actually *1
Command to DRQ (Sector Read at Ready state)	4 ms (max.)
Command to DRQ (Sector Write at Ready state)	700 μs (max.)
Data transfer cycle end to ready (Sector write)	2 ms (typ.), 200 ms (max.)
Auto Power down time	1.5s (min.), 1.8s (typ.)

Notes:

1. The actual transfer rate is measured under ATA PIO mode 4 with single cycle time as 120ns.

ELECTRICAL SPECIFICATION

SYMBOL	PARAMETER	MIN	MAX	TYP	UNIT
V_{IN} , V_{OUT}	All input / output voltage	−0.3	V_{CC}+ 0.3	—	V
V_{CC}	Power Supply Voltage (Absolute Maximum Ratings)	−0.6	6.0	—	V
V_{CC}	Power Supply Voltage (Recommended Operation Condition)	4.5	5.5	5.0	V
		3.135	3.465	3.3	V
T_{opr}	Operating Temperature	−40	85	—	°C
T_{stg}	Storage Temperature	−45	90	—	°C

Input Leakage Current

Type	SYMBOL	PARAMETER	CONDIDTION	MIN	MAX	TYP	UNIT	NOTES
IxZ	IL	Input leakage current	V_{IH}=Vcc / V_{IL}=GND	-1	1	—	μA	*1
IxU	RPU1	Pull Up Resistor	Vcc = 5.0V	50	500	—	kΩ	*1
IxD	RPD1	Pull Down Resister	Vcc = 5.0V	50	500	—		*1

Notes:

1. x refers to the characteristics described in section “DC Characteristics (Input Characteristics)”. For example, I1U indicates a pull up resister with a type 1 input characteristics.

Output Drive Type

Type	OUTPUT TYPE	VALID CONDITIONS	NOTES
OTx	Totempole	I_{OH} & I_{OL}	*1
OZx	Tri-State N-P Channel	I_{OH} & I_{OL}	*1
OPx	P-Channel only	I_{OH} Only	*1
ONx	N-Channel only	I_{OL} Only	*1

Notes:

1. x refers to the characteristics described in section “DC Characteristics (Output Drive Characteristics)”. For example, OT1 refers to Totempole output with a type 1 Output drive characteristics.

DC CHARACTERISTICS (V_{CC} = 3.3 V ± 5%, 5 V ± 0.5V, Ta = -40°C~85°C)

SYMBOL	PARAMETER	MIN	MAX	TYP.	UNIT	TEST CONDITIONS
I_{LI}	Input leakage current	—	1	—	μA	—
I_{LO}	Output leakage current	—	1	—	μA	V_{OUT} = high impedance
$-I_{PU}$	Pull-up current (Resistivity)	—	—	43 (75)	μA (kΩ)	V_{FORCE} = 3.3V
$-I_{PD}$	Pull-down current (Resistivity)	—	—	−43 (75)	μA (kΩ)	V_{FORCE} = 0V
I_{CCS}	Power down mode current	— —	1.5 2.0	1.0 1.2	mA	V_{CC} = 3.3V V_{CC} = 5V
I_{CCO}	Operating current @ 3.3V Write operation Read operation	— —	— —	25 21	mA	V_{CC} = 3.3V operation
	Operating current @ 5V Write operation Read operation	— —	— —	28 23	mA	V_{CC} = 5V operation

Input Characteristics

Type	SYMBOL	PARAMETER	MIN	MAX	TYP	UNIT	CONDITION
1	V_{IH}	Input High Voltage CMOS	2.0 2.0	—	—	V	V_{CC} = 3.3 V V_{CC} = 5 V
	V_{IL}	Input Low Voltage CMOS	—	1.0 1.0	—		V_{CC} = 3.3 V V_{CC} = 5 V
2	V_{IH}	Input High Voltage	2.0 2.0	—	—		V_{CC} = 3.3 V V_{CC} = 5 V
	V_{IL}	Input Low Voltage CMOS	—	1.0 0.8	—		V_{CC} = 3.3 V V_{CC} = 5 V
3	V_{T+}	Input Low to High threshold Schmitt trigger	—	2.5 2.5	2.1 2.1		V_{CC} = 3.3 V V_{CC} = 5 V
	V_{T-}	Input High to Low threshold Schmitt trigger	0.9 0.9	—	1.2 1.2		V_{CC} = 3.3 V V_{CC} = 5 V
	ΔVt	Hysteresis voltage	0.5 0.8				V_{CC} = 3.3 V V_{CC} = 5 V
4	V_{T+}	Input Low to High threshold Schmitt trigger	—	2.3 2.0	2.1 1.8		V_{CC} = 3.3 V V_{CC} = 5 V
	V_{T-}	Input High to Low threshold Schmitt trigger	1.0 0.8	—	1.2 1.1		V_{CC} = 3.3 V V_{CC} = 5 V
	ΔVt	Hysteresis voltage	0.5 0.8				V_{CC} = 3.3 V V_{CC} = 5 V

Output Drive Characteristics

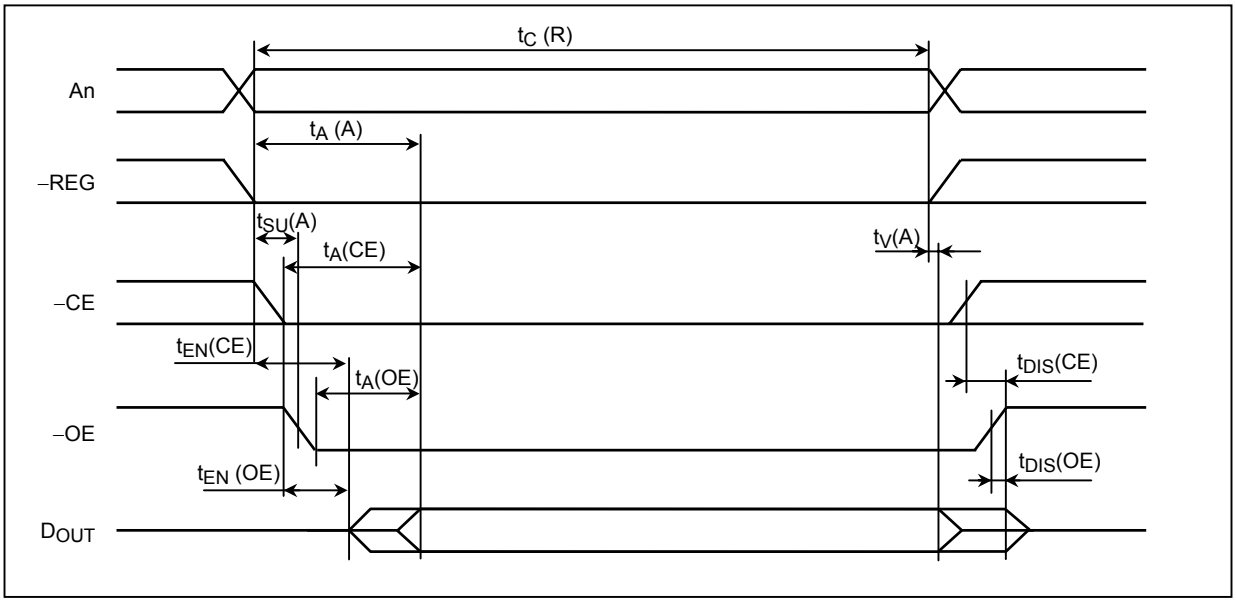
Type	SYMBOL	PARAMETER	MIN	MAX	TYP	UNIT	CONDITION
1	V_{OH}	Output High Voltage	V_{CC} − 0.8	—	—	V	I_{OH} = −4mA
	V_{OL}	Output Low Voltage	—	Gnd + 0.4	—		I_{OL} = 4mA

AC CHARACTERISTICS (V_{CC} = 3.3 V ± 5%, 5 V ± 0.5V, Ta = -40°C~85°C)

Attribute Memory Read AC Characteristics

SYMBOL	PARAMETER	MIN	MAX	TYP	UNIT	NOTES
t_C (R)	Read cycle time	250	—	—	ns	
t_A (A)	Address access time	—	250	—		
t_A (CE)	–CE access time	—	250	—		
t_A (OE)	–OE access time	—	125	—		
t_{DIS} (CE)	Output disable time (–CE)	—	100	—		
t_{DIS} (OE)	Output disable time (–OE)	—	100	—		
t_{EN} (CE)	Output enable time (–CE)	5	—	—		
t_{EN} (OE)	Output enable time (–OE)	5	—	—		
t_V (A)	Data valid time (A)	0	—	—		
t_{SU} (A)	Address setup time	30	—	—		

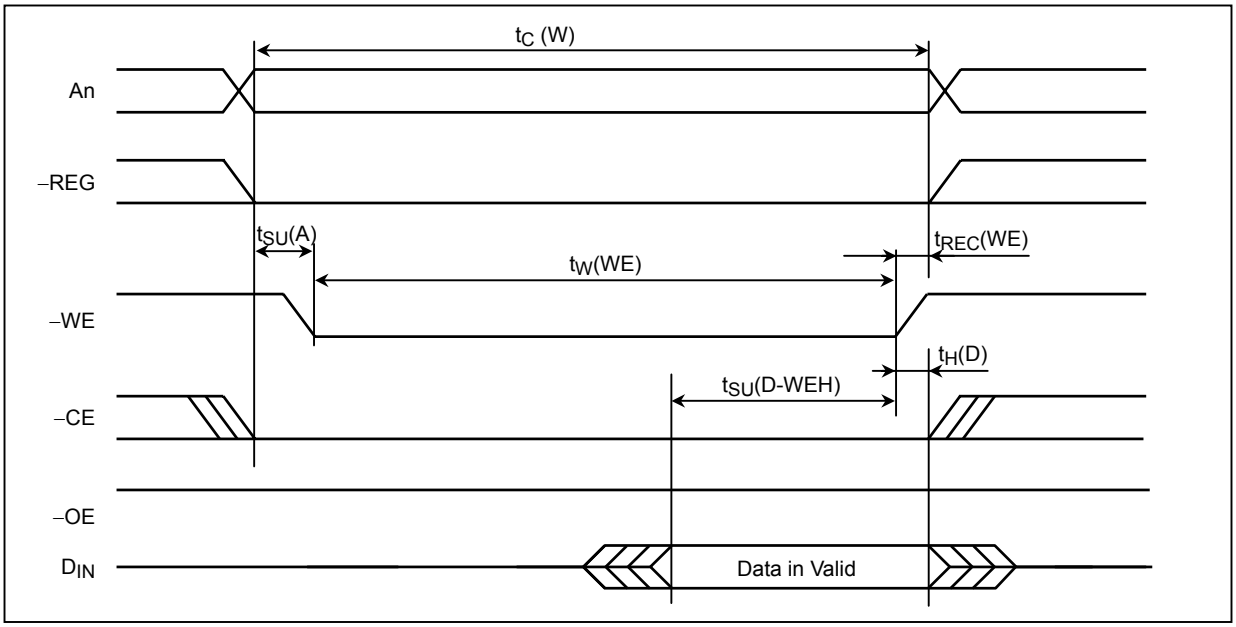
Attribute Memory Read Timing



Attribute Memory Write AC Characteristics

SYMBOL	PARAMETER	MIN	MAX	TYP	UNIT	NOTES
t_C (W)	Write cycle time	250	—	—	ns	
t_W (WE)	Write pulse time	150	—	—		
t_{SU} (A)	Address setup time	30	—	—		
t_{SU} (D-WEH)	Data setup time (–WE)	80	—	—		
t_H (D)	Data hold time	30	—	—		
t_{REC} (WE)	Write recover time	30	—	—		

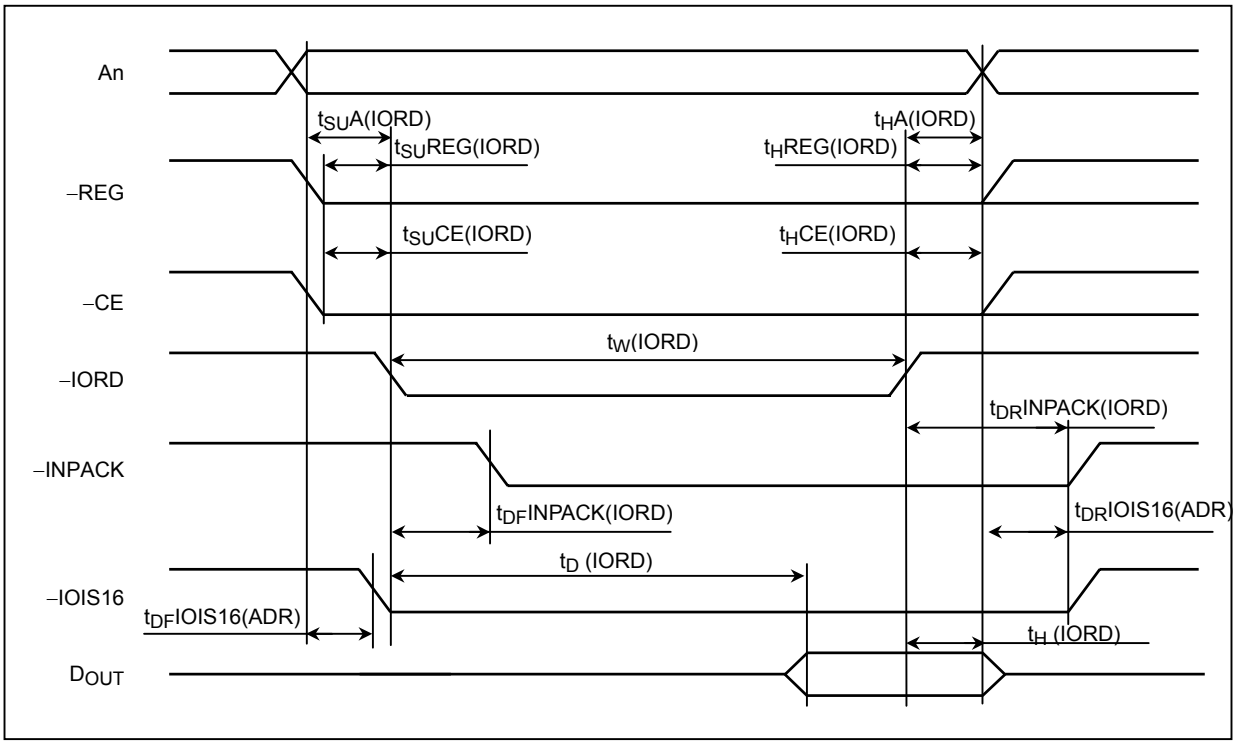
Attribute Memory Write Timing



I/O Access Read AC Characteristics

SYMBOL	PARAMETER	MIN	MAX	TYP	UNIT	NOTES
t_D (IORD)	Data delay after –IORD	—	100	—	ns	
t_H (IORD)	Data hold following –IORD	0	—	—		
t_W (IORD)	–IORD pulse width	165	—	—		
t_{SU}A (IORD)	Address setup before –IORD	70	—	—		
t_HA (IORD)	Address hold following –IORD	20	—	—		
t_{SU}CE (IORD)	–CE setup before –IORD	5	—	—		
t_HCE (IORD)	–CE hold following –IORD	20	—	—		
t_{SU}REG (IORD)	–REG setup before –IORD	5	—	—		
t_HREG (IORD)	–REG hold following –IORD	0	—	—		
t_{DF}INPACK (IORD)	–INPACK delay failing from –IORD	0	45	—		
t_{DR}INPACK (IORD)	–INPACK delay rising from –IORD	—	45	—		
t_{DF}IOIS16 (ADR)	–IOIS16 delay failing from address	—	35	—		
t_{DR}IOIS16 (ADR)	–IOIS16 delay rising from address	—	35	—		

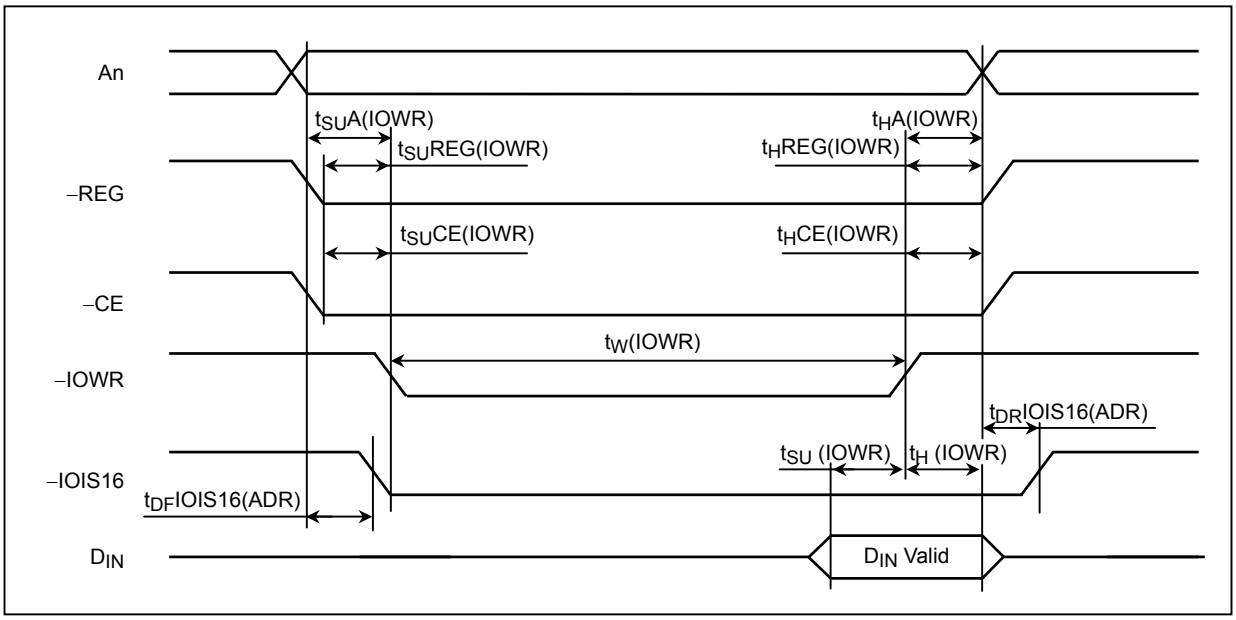
I/O Access Read Timing



I/O Access Write AC Characteristics

SYMBOL	PARAMETER	MIN	MAX	TYP	UNIT	NOTES
t_{SU} (IOWR)	Data setup before –IOWR	60	—	—	ns	
t_H (IOWR)	Data hold following –IOWR	30	—	—		
t_W (IOWR)	–IOWR pulse width	165	—	—		
t_{SU}A (IOWR)	Address setup before –IOWR	70	—	—		
t_HA (IOWR)	Address hold following –IOWR	20	—	—		
t_{SU}CE (IOWR)	–CE setup before –IOWR	5	—	—		
t_HCE (IOWR)	–CE hold following –IOWR	20	—	—		
t_{SU}REG (IOWR)	–REG setup before –IOWR	5	—	—		
t_HREG (IOWR)	–REG hold following –IOWR	0	—	—		
t_{DF}IOIS16 (ADR)	–IOIS16 delay failing from address	—	35	—		
t_{DR}IOIS16 (ADR)	–IOIS16 delay rising from address	—	35	—		

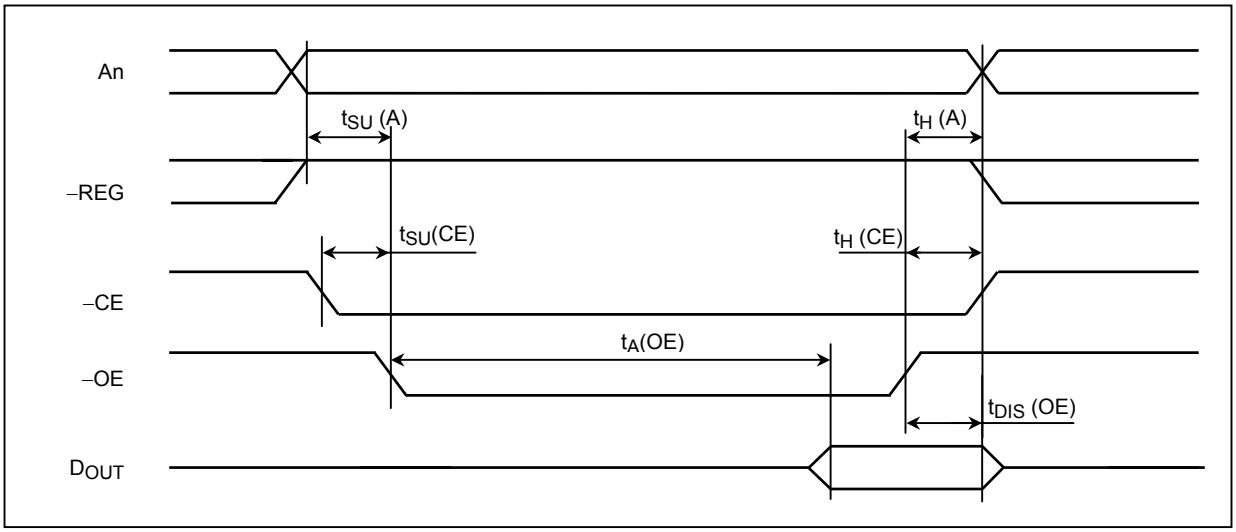
I/O Access Write Timing



Common Memory Access Read AC Characteristics

SYMBOL	PARAMETER	MIN	MAX	TYP	UNIT	NOTES
t_A (OE)	−OE access time	—	125	—	ns	
t_{DIS} (OE)	Output disable time (−OE)	—	100	—		
t_{SU} (A)	Address setup time	30	—	—		
t_H (A)	Address hold time	20	—	—		
t_{SU} (CE)	−CE setup before −OE	0	—	—		
t_H (CE)	−OE hold following −OE	20	—	—		

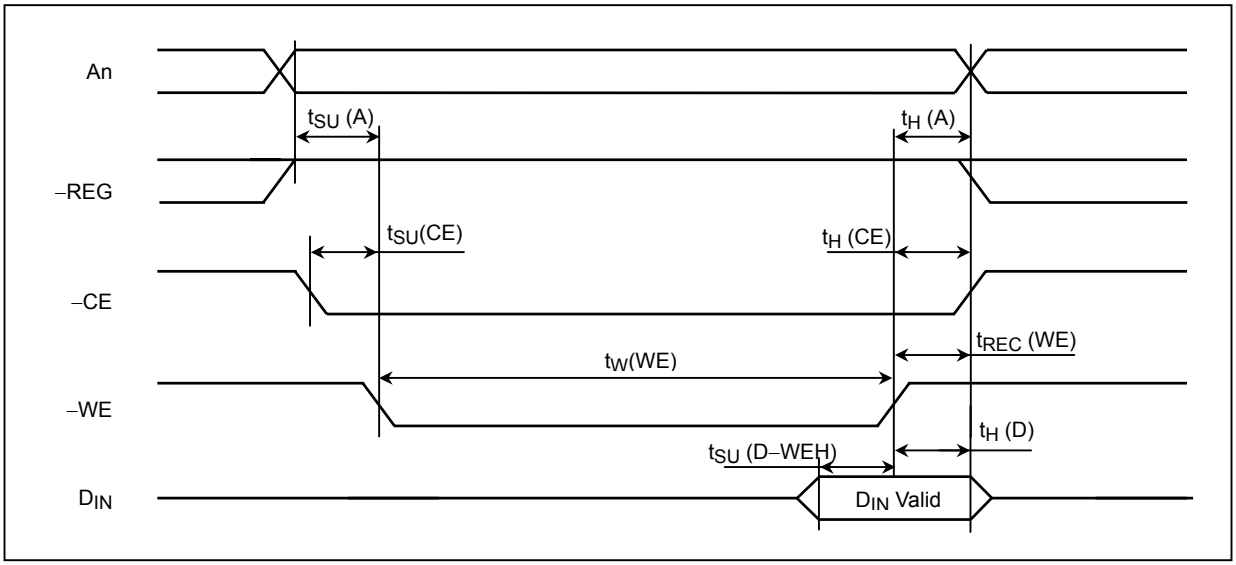
Common Memory Access Read Timing



Common Memory Access Write AC Characteristics

SYMBOL	PARAMETER	MIN	MAX	TYP	UNIT	NOTES
t_{SU} (D–WEH)	Data setup before –WE	80	—	—	ns	
t_H (D)	Data hold following –WE	30	—	—		
t_W (WE)	Write pulse width	150	—	—		
t_H (A)	Address hold time	20	—	—		
t_{SU} (A)	Address setup time	30	—	—		
t_{SU} (CE)	–CE setup time	0	—	—		
t_{REC} (WE)	Write recover time	30	—	—		
t_H (CE)	–CE hold following –WE	20	—	—		

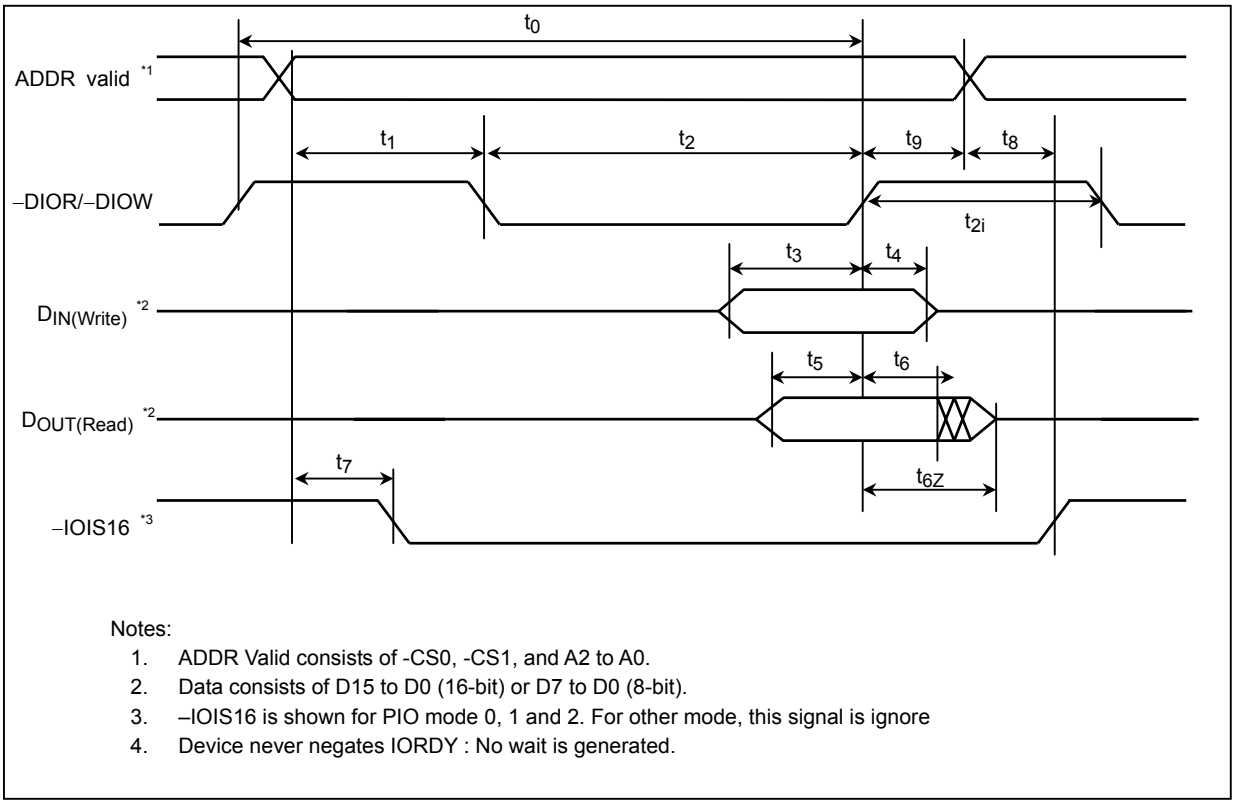
Common Memory Access Write Timing



True IDE Mode IO Read/Write AC Characteristics

SYMBOL	PARAMETER	MIN	MAX	TYP	UNIT	NOTES
t_0	Cycle time	120	—	—	ns	
t_1	Address valid to –DIOW/–DIOR setup	25	—	—		
t_2	–DIOW/–DIOR	70	—	—		
t_2	–DIOW/–DIOR Register (8bit)	70	—	—		
t_{2i}	–DIOW/–DIOR recoverry time	25	—	—		
t_3	–DIOW data setup	20	—	—		
t_4	–DIOW data hold	10	—	—		
t_5	–DIOR data setup	20	—	—		
t_6	–DIOR data hold	5	—	—		
t_{6z}	–DIOR data tristate	—	30	—		
t_7	Address valid to –IOIS16 assertion	—	35	—		
t_8	Address valid to –IOIS16 released	—	35	—		
t_9	–DIOW/–DIOR to address valid hold	10	—	—		

True IDE Mode IO Access Read/Write Timing



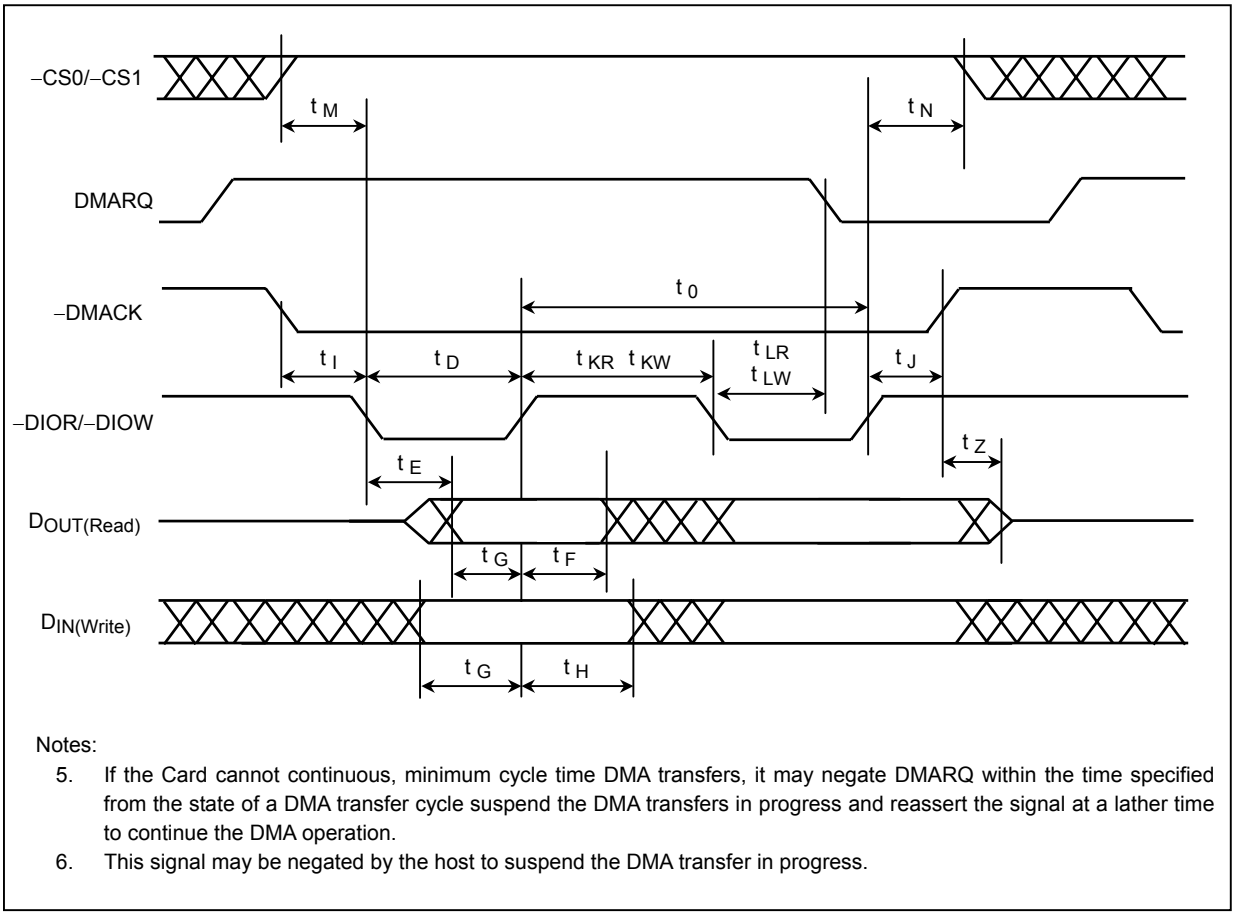
Notes:

1. ADDR Valid consists of -CS0, -CS1, and A2 to A0.
2. Data consists of D15 to D0 (16-bit) or D7 to D0 (8-bit).
3. –IOIS16 is shown for PIO mode 0, 1 and 2. For other mode, this signal is ignore
4. Device never negates IORDY : No wait is generated.

True IDE Mode Multiword DMA Read/Write AC Characteristics

SYMBOL	PARAMETER	MIN	MAX	TYP	UNIT	NOTES
t_0	Cycle time	120	—	—	ns	
t_D	–DIOR/–DIOW assert width	70	—	—		
t_E	–DIOR data access	—	50	—		
t_F	–DIOR data hold	5	—	—		
t_G	–DIOW/–DIOR data setup	20	—	—		
t_H	–DIOW data hold	10	—	—		
t_I	–DMACK to –DIOR/–DIOW setup	0	—	—		
t_J	–DIOR/–DIOW to DMACK hold	5	—	—		
t_{KR}	–DIOR negated width	25	—	—		
t_{KW}	–DIOW negated width	25	—	—		
t_{LR}	–DIOR to DMARQ delay	—	35	—		
t_{LW}	–DIOW to DMARQ delay	—	35	—		
t_M	–CS0/–CS1 valid to –DIOR/–DIOW	25	—	—		
t_N	–CS0/–CS1 hold	10	—	—		
t_Z	–DMACK to read data released	—	25	—		

True IDE Mode DMA Access Read/Write Timing



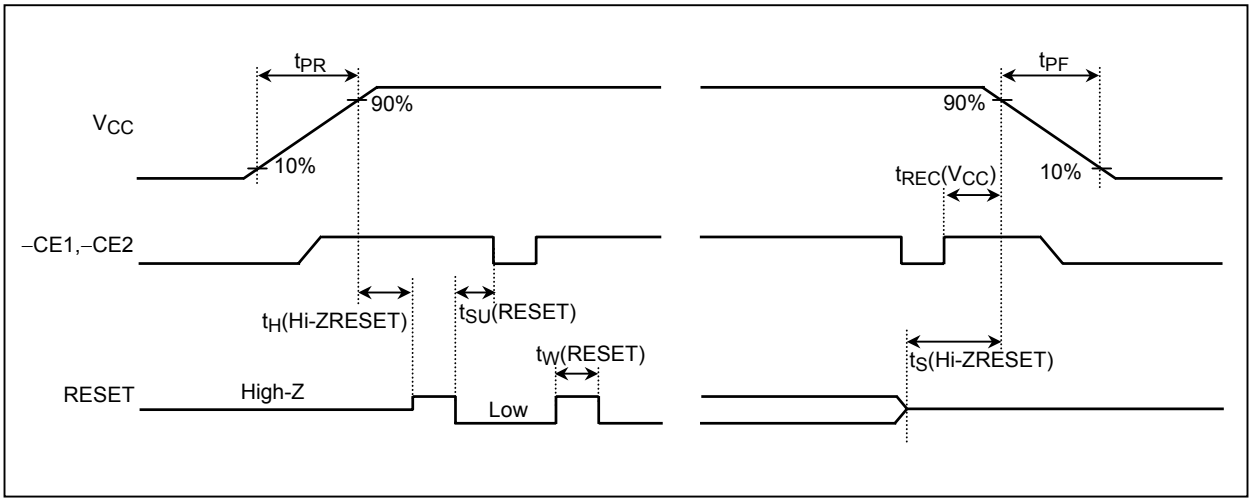
Notes:

5. If the Card cannot continuous, minimum cycle time DMA transfers, it may negate DMARQ within the time specified from the state of a DMA transfer cycle suspend the DMA transfers in progress and reassert the signal at a lather time to continue the DMA operation.
6. This signal may be negated by the host to suspend the DMA transfer in progress.

Reset Characteristics (only Memory Card Mode or I/O Card Mode)

SYMBOL	PARAMETER	MIN	MAX	TYP	UNIT	NOTES
t_{SU} (RESET)	Reset setup time	100	—	—	ms	
t_{REC} (VCC)	–CE recover time	1	—	—	μs	
t_{PR}	VCC rising up time	0.1	100	—	ms	
t_{PF}	VCC falling down time	3	300	—	ms	
t_W (RESET)	Reset pulse width	10	—	—	μs	
t_H (Hi-ZRESET)		1	—	—	ms	
t_S (Hi-ZRESET)		0	—	—	ms	

Hardware Reset Timing

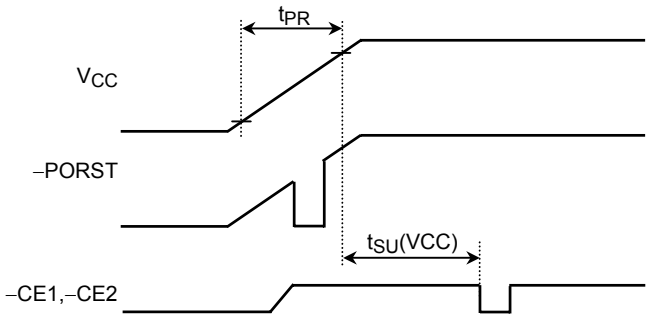


Power on Reset Characteristics

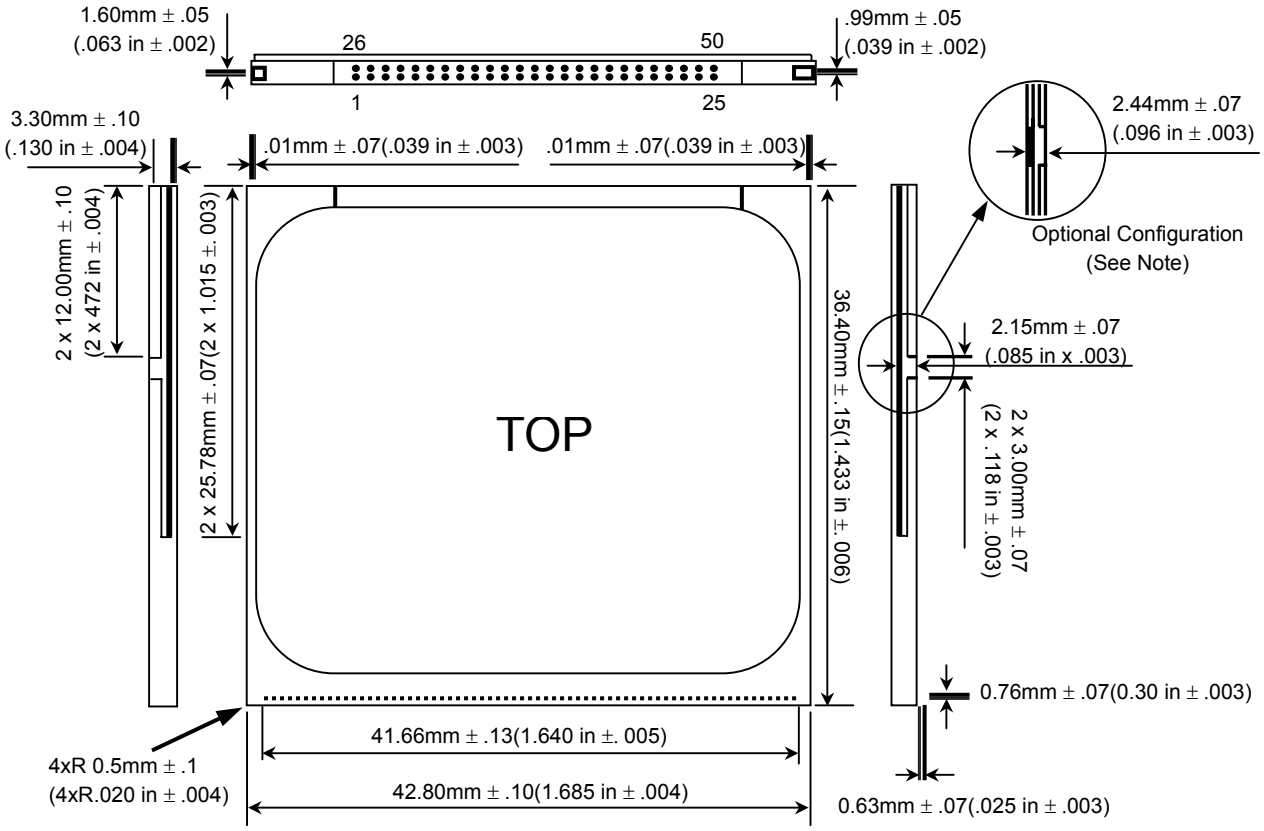
Power on reset sequence must need by –PORST at the rising of V_{CC}.

SYMBOL	PARAMETER	MIN	MAX	TYP	UNIT	NOTES
t_{SU} (VCC)	–CE setup time	100	—	—	ms	
t_{PR}	VCC rising up time	0.1	100	—	ms	

Power on Reset Timing



Package Dimensions



Note:	The optional notched configuration was shown in the CF Specification Rev.1.0. In Specification Rev. 1.2. The notch was removed for ease of tooling. This optional configuration can be used but it is not recommended.

Type Ⅰ CompactFlash Storage Card Dimensions

Attention for Card Use

- In the reset or power off, the information of all registers is cleared.
- Notice that the card insertion/removal should not be executed during host is active, if the card is used in True IDE mode.
- After the card hard reset, soft reset, or power on reset, ATA reset, command applied the card cannot access during READY pin is “low” level. Flash card can’t be operated in this case.
- Before the card insertion V_{CC} cannot be supplied to the card. After confirmation that –CD1, –CD2 pins are inseted, supply V_{CC} to the card.
- –OE must be kept at the V_{CC} level during power on reset in memory card mode and I/O card mode. –OE must be kept constantly at the GND level in True IDE mode.
- Do not turn off the power or remove THNCFxxxxDGI Series from the slot before read/write operation is complete. Avoid using THNCFxxxxDGI Series when the battery is low. Power shortage, power failure and/or removal of THNCFxxxxDGI Series from the slot before read/write operation is complete may cause malfunction of THNCFxxxxDGI Series, data loss and/or damage to data.
- Routine performance of backing-up data (or taking back-up of data) is strongly recommended.

RESTRICTIONS ON PRODUCT USE

000707EBA

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